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Comparative Analysis of CMOS-based D-type Flip-Flop Architectures for High-Performance VLSI Applications Using 45-nm CMOS Technology

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Abstract

High performance VLSI (very large-scale integration) is an essential electronic technology required for space missions and scientific advancements. The only source of reliance for the VLSI designer is the data storage devices designated as flip-flops, which are widely used in semiconductor memory devices as well as for data processing and storage in the telecommunication fields. In this paper, the four D-type flip-flop architectures of CMOS-based D-type flip-flops, such as D-type flip-flops using traditional technology (DFF-T), D-type flip-flops with De-Morgan's law (DFF-DL), D-type flip-flops with transmission gates (DFF-TG), and D-type flip-flops with five transistors (DFF-F), have been designed and constructed. The analytical simulations of the schematics and equivalent layouts of these four architectures are implemented using 45-nm complementary metal-oxide-semiconductor (CMOS) technology. With cadence virtuoso design software, the performance investigation of the four D-type flip-flop architectures is compared in terms of layout area, transistor counts, average power consumption, rise time, fall time, and propagation delay. The DFF-F technologies have modestly compact design goals in order to reduce production costs and achieve faster processing speeds with fewer transistors.

A. Introduction

Flip-flops are the data storage devices which are used in a wide range of applications, such as semiconductor memory devices, telecommunication sector, integrated circuits**,** spaceships, etc. There are several varieties of flip-flops. Among these, the D-type flip-flop is widely used because it catches the value of the data input (D) during a certain preset section of the control clock pulse (leading or trailing edge of the clock) and its output is unaffected at other portions of the clock. In terms of timing, the delay caused by D-type flip-flops consumes a significant portion of the cycle time as the operating frequency increases. Minimizing propagation delay requires different strategies depending on the circuit level, architecture, layout, and manufacturing technology. This is an efficient method for designing a flip-flop with fewer transistors for a low propagation delay. There are several D-type flip-flop topologies in the literature. Fewer transistors are employed in the proposed technique, which occupies less area and thus consumes less power than a standar D-type flip-flop with more transistors.

D-type flip-flops are implemented in Tanner Tool-Version.16 using 250-nm CMOS technology, and the high-speed D-type flip-flop design is compared with conventional D-type flip-flops in terms of chip size area, aspect ratio, transistor count, and propagation delay [1]. Nine D-type Flip-Flop (DFF) designs were constructed in 28 nm FDSOI with a target subthreshold supply voltage of 200 mV [2]. SPICE software environment is used to create designs of CMOS-based D-type flip-flop circuits employing forced nMOS-stacking, LCNT (leakage-controlled nMOS transistor), and LECTOR (leakage-controlled transistor) using different low-power strategies based on TSMC 180nm CMOS technology [3]. The Conditional Pass Logic Static D-Flip-Flop (CPLSDFF) and Conditional Pass Logic Dynamic D-Flip-Flop (CPLDDFF) topologies are built using SPICE and 130 nm IBM transistor technology, resulting in a 27% and 22% reduction in silicon area [4]. The D-type flip-flop is designed with nine-tracks functioning at 0.8 V and a poly-pitch of 0.24 nm, with the library built at 45 nm in Cadence Virtuoso-v6.1.6. [5]. A SET D-type flip-flop with 5-transistors is presented utilizing several scaling methods, including 180 nm, 90 nm, 70 nm, and 50 nm. In this research paper, power dissipation and area are compared [6]. The D flip-flop with only 8 transistors has been modified to optimize total capacitance during operation, resulting in lower average power dissipation. Cadence tools in 0.18 μm technology are used for characterization [7].

Therefore, it's important to choose fundamental components wisely,i.e., flip-flops, is vital to achieving the essential characteristics that benefit the larger system [8]. Making sure these considerations in mind, the following contributions are provided in this paper. The first step is to create four different D-type flip-flop circuits and observe their outputs. The second step is to analyze the results from the first step and to check which circuit provides the least rise time, fall time, average power consumption, chip size and propagation delay. The final step is to conclude the better D-type flip-flop circuit in terms of rise time, fall time, power consumption, chip size and propagation delay.

The remaining section of the paper is structured as follows: Section B discusses to implementation of CMOS-based D-type flip-flop, static, dynamic, and short-circuit power consumption, as well as process design and simulation parameters in the Cadence environment. Section C shows the simulation results for

the performance parameters (transistor counts, layout area, power consumption, rise time, fall time, and delay) of four CMOS-based D-type flip-flop topologies. This section also includes some discussion on comparison of four CMOS-based D-type flip-flop topologies (in terms of performance characteristics). Finally, Section D ends up with the conclusion.

B. Implementation of D-type flip-flop using CMOS technology

There are four methods of implementation of D-type flip-flops that are compared in this research work. The first method is D-type flip-flops using the traditional technique (DFF_T) (which is illustrated in Figure 1), the second method is D-type flip-flop with De-Morgan's Law (DFF-DL) (which is shown in Figure 2), the third method is D-type flip-flop with transmission gates (DFF-TG) (which is demonstrated in Figure 3), and the last is D-type flip-flops with five transistors (DFF-F) (which is demonstrated in Figure 4). All methods are constructed with 45-nm CMOS technology with NAND gates only, which are universal gates [9].

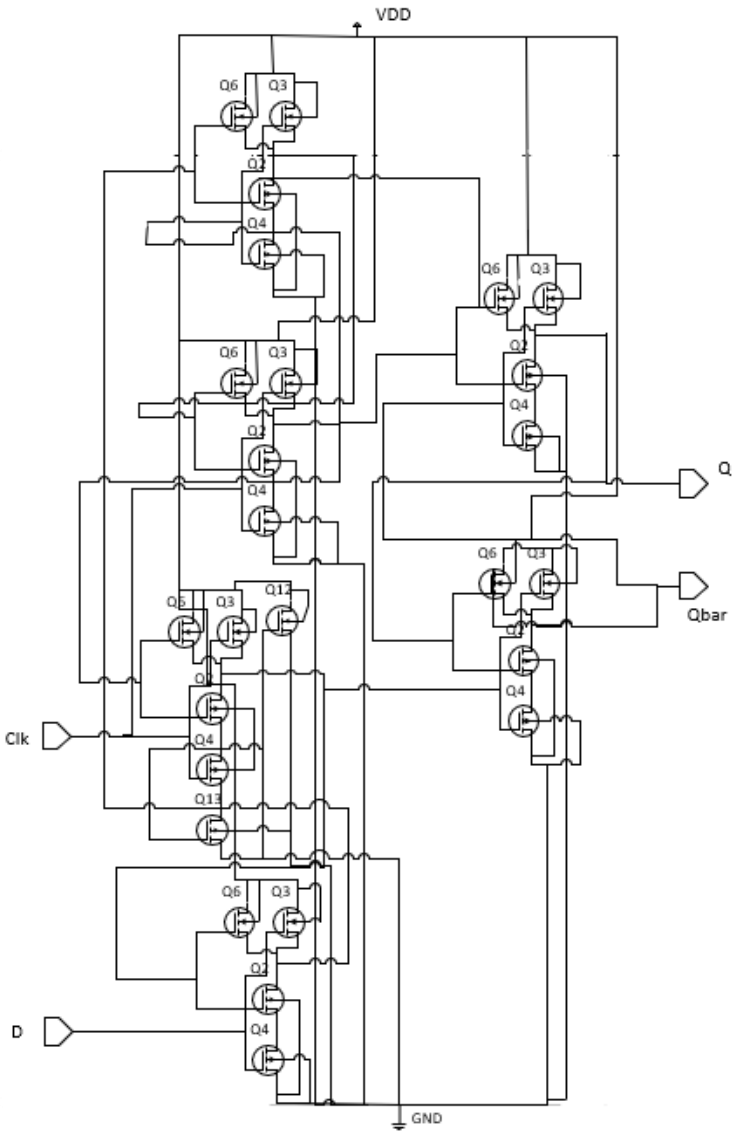


Figure 1. Schematic diagram of D-type flip-flop using traditional technique(DFF-T)

D-type flip-flop using traditional method (DFF-T) is built with 26 transistors (13 PMOS and 13 NMOS). The cicuit arrangement of the first method is shown in Figure 1. As a result, PMOS and NMOS contributed equally to the overall operation of the circuit. Supply voltages (V_{DD}) have essentially been scaled in order to achieve the goal of low power consumption. The proposed DFF-T design has two inputs ("D" and "Clk") and two outputs, where "Q" stands for the circuit's output, "Qbar" for the output bar.

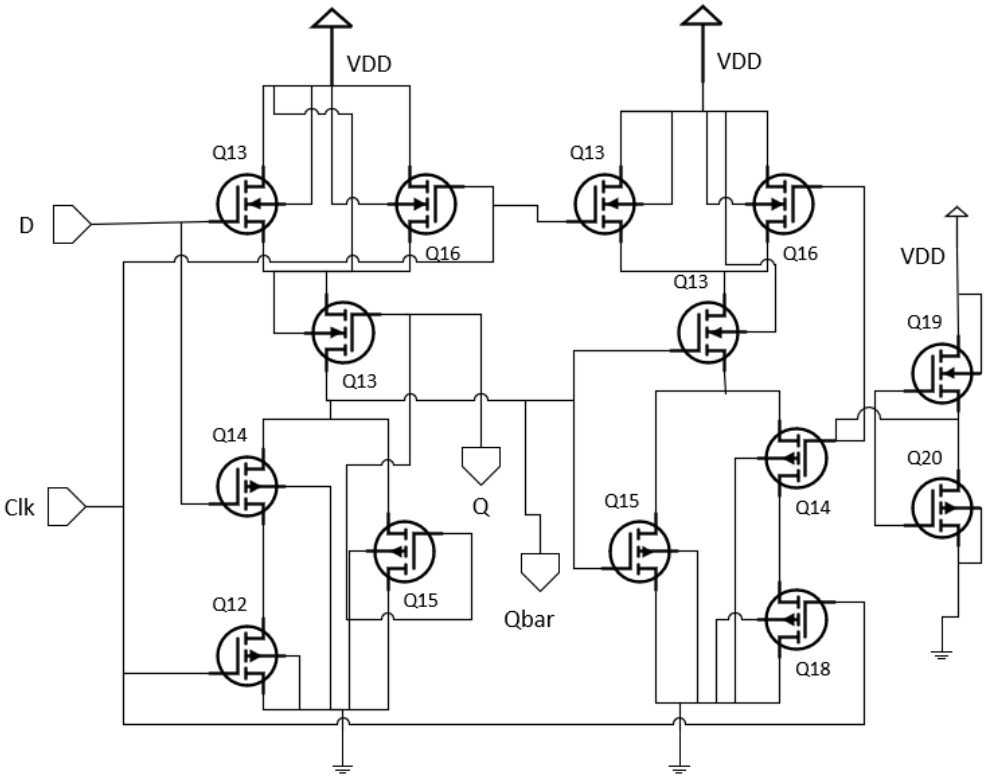


Figure 2. Schematic diagram of D-type flip-flop with De-Morgan's law (DFF-DL)

D-type flip-flop with De-Morgan's law (DFF-DL) is constructed with 14 transistors (7 PMOS and 7 NMOS), which is shown in Figure 2[12]. The proposed DFF-T design has two inputs ("D" and "Clk") and two outputs, where "Q" stands for the circuit's output, "Qbar" for the output bar.

D-type flip-flop with transmission gates (DFF-TG) is constructed with 10 transistors (5 PMOS and 5 NMOS), which is illustrated in Figure 3 [13].The proposed DFF-T design has two inputs ("D" and "Clk") and two outputs, where "Q" stands for the circuit's output, "Qbar" for the output bar. Rather than standard CMOS pull-up and pull-down networks, transmission gates can be used to build logic circuits. Such circuits may frequently be made smaller, which is an essential issue in silicon implementations.

D-type flip-flop using five transistors method is implemented with 5 transistors (2 PMOS and 3 NMOS). The circuit arrangement of D-type flip-flop using five transistors method is shown in Figure 4[14]. The proposed DFF-T design has two inputs ("D" and "Clk") and two outputs, where "Q" stands for the circuit's output, "Qbar" for the output bar.

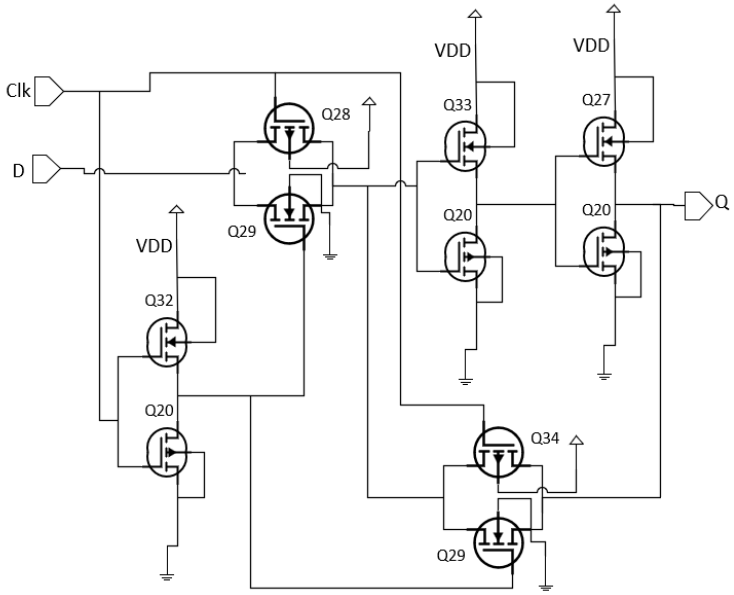


Figure 3. Schematic diagram of D-type flip-flop with transmission gates (DFF-TG)

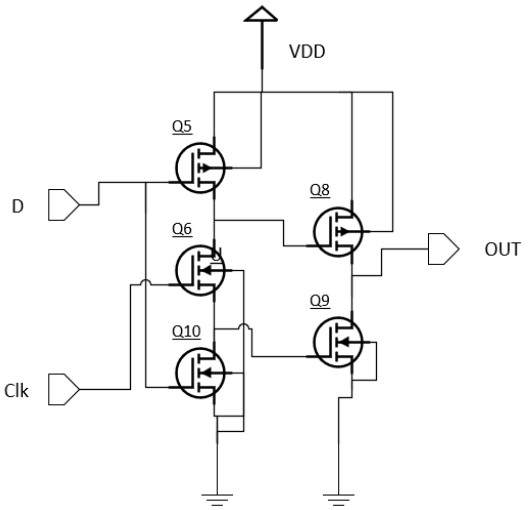


Figure 4. Schematic diagram of D-type flip-flop using five transistors (DFF-F)

Static, dynamic and short-circuit power consumption

There are three main sources of power consumption. They are static, dynamic and short-circuit power consumption [10]. The following equations are used in the calculation of power consumption in this paper.

$$\text{Power dissipation, } P = I \times V_{dd} \quad (1)$$

$$\text{Propagation delay} = 0.69\, R_{eq} \times C_L \quad (2)$$

$$\text{Power Delay Product} = \text{Average power Consumption} \times \text{Propagation Delay} \quad (3)$$

$$P_{avg} = p_t (C_L V * V_{dd} * f_{clk}) + I_{sc} * V_{dd} + I_{leakage} * V_{dd} \quad (4)$$

Where,

C_L = Load capacitance

R_{eq} = equivalent resistance

P_{avg} =Average power Consumption

The three main sources of power in very large-scale integrated circuits are represented by the above equation. The first term represents the dynamic or switching power dissipation. The second term denotes the short-circuit power dissipation path directly. Leakage power is shown in the third phrase. The most power is consumed by dynamic power, whose output is related to V^2_{dd}. Therefore, the best technique to decrease the design's power dissipation is to lessen the supply voltage. The speed of the intended circuit is decreased. Clock frequency reduction is another method for reducing dynamic power [11].

Design and simulation parameters used in the Cadence environment

In the complementary metal oxide semiconductor (CMOS) circuit, N-channel MOSFET and P-channel MOSFET transistors are used from the gpdk045 library of the Cadence Virtuoso design tool [15]. Table 1 presents the design and simulation parameters including the library and cell view names used for four types of proposed design techniques.

Table 1. Cadence Virtuoso environment's design and simulation parameters

Library Name	Cell View Name	Properties	Temperature
gpdk045	pmos1v	Total Width = 120 nm, Length = 45 nm	27˚C
gpdk045	nmos1v	Total Width = 120 nm, Length = 45 nm	27˚C
gpdk045	pmos2v	Total Width = 320 nm, Length = 150 nm	27˚C
gpdk045	nmos2v	Total Width = 320 nm, Length = 150 nm	27˚C
analogLib	vpulse (as Clock input signal)	voltage1=0, voltage2=1.8V, period =1µs, pulse width= 500ns	27˚C
analogLib	vpulse (as D input signal)	voltage1=0, voltage2=1.8V,period =700ns, pulse width= 250ns	27˚C
analogLib	vdc	DC voltage =1.8 V	27˚C
analogLib	vdd	DC voltage =1.8 V	27˚C
analogLib	vss		27˚C

C. Result and Discussion

The schematic diagrams, transient characteristics, and layout designs of all CMOS-based D-type flip-flop architectures presented in this research work are implemented with 45-nm CMOS technology in a cadence virtuoso software environment. Their performance parameters, such as chip size area, transistor count, average power consumption, rise time, fall time, and propagation delay, were calculated and compared with each other using the ADE-XL simulator and the Monte-Carlo sampling method. All methods are operated with a timing duration of 10 µs, temperature of 27˚C and a 1.8 V power supply.

Design of the DFF-T technique

The DFF-T design is built with 26 transistors (13 PMOS and 13 NMOS). The circuit used in the DFF-T approach is made up of a pull-up network (i.e., PMOS)

and a pull-down network (i.e., NMOS). Thus, both PMOS and NMOS made an equal contribution to the circuit's overall functioning. Supply voltages (V_{dd}) have essentially been scaled in order to achieve the goal of low power consumption.

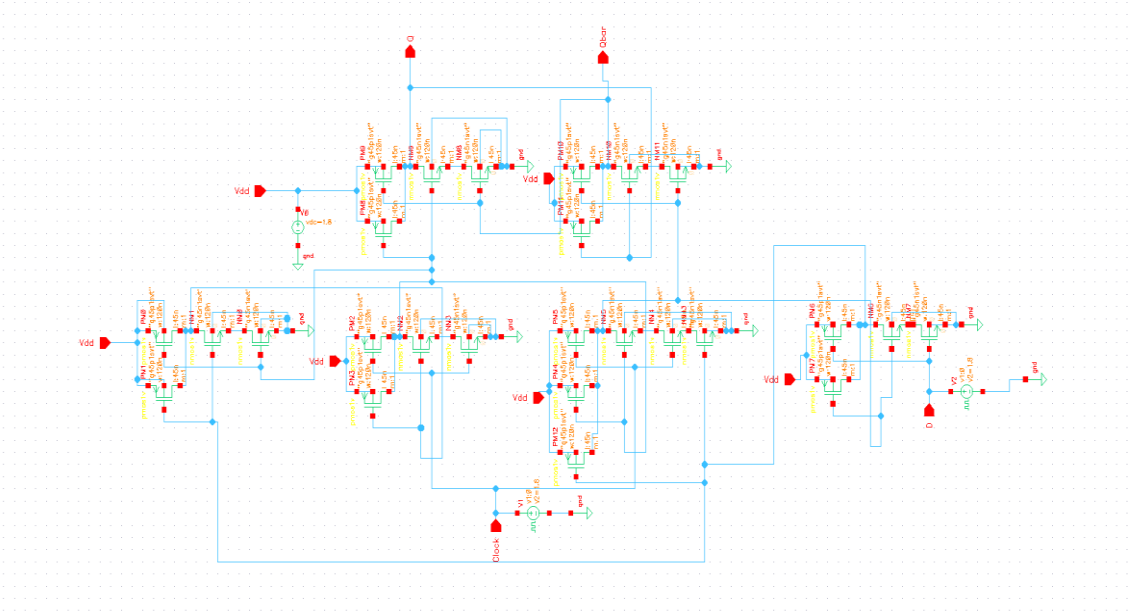


Figure 5. Circuit representation of the DFF-T Technique

The DFF-T design minimizes both the circuit's average power consumption and delay. The DFF-T design has two inputs and two outputs, as illustrated in Figure 5, where "Q" stands for the circuit's output, "Qbar" for the complement of the output, and "D" and "Clock" for the inputs. The dimensions of the transistors are as follows.

NMOS transistors: W = 120 nm, L= 45 nm
PMOS transistors: W = 120 nm, L= 45 nm

The DFF-DL technique's design

The overall circuit in the DFF-DL method is made up of the pull-up network (PMOS) and the pull-down network (NMOS) [8-9]. As a result, PMOS and NMOS both contributed equally to the circuit's total performance. Low power consumption was primarily achieved by adjusting supply voltages (V_{dd}). The proposed DFF-DL consists of fourteen transistors (seven PMOS and seven NMOS). The proposed design reduces both the circuit's average power consumption and delay. Figure 6 shows the suggested DFF-DL architecture with two inputs and two outputs. In Figure 6, "Q" represents the circuit's output, "Q_{bar}" its counterpart, and the inputs "D" and "CLK". The transistors have the following dimensions:

W = 320 nm, L = 150 nm for NMOS transistors.
W = 320 nm, L = 150 nm for PMOS transistors.

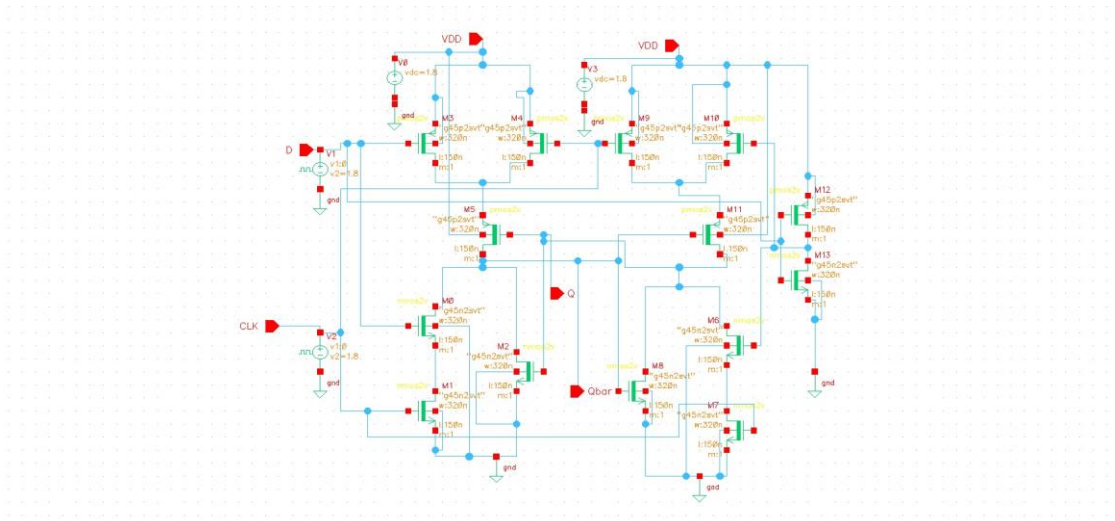


Figure 6. Circuit representation of the DFF-DL Technique

The DFF-TG technique's design

Figure 7 demonstrates how the proposed DFF-TG technique is implemented using ten transistors (five PMOS and five NMOS), each with two inputs and two outputs [9].

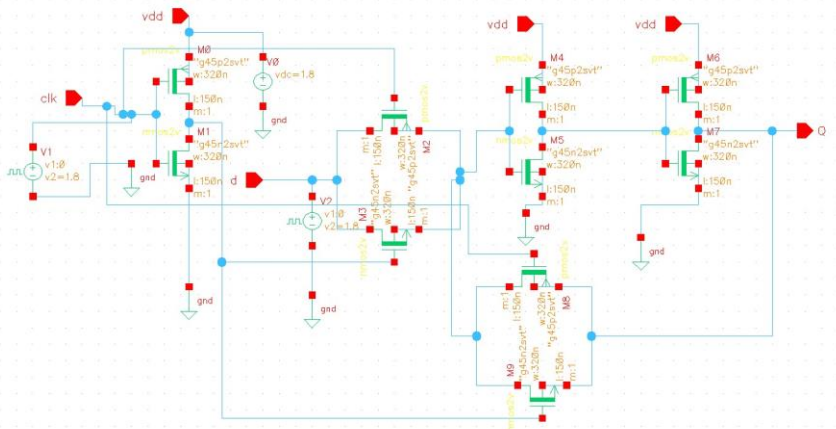


Figure 7. Circuit representation of the DFF-TG Technique

In comparison to the DFF-DL circuit, the DFF-TG approach reduces the delays, power delay product, chip size, and average power of the proposed design [10]. To reduce leakage and power consumption, this circuit employs transmission gate transistors. The transistors possess the following dimensions:

W = 320 nm, L = 150 nm for NMOS transistors.
W = 320 nm, L = 150 nm for PMOS transistors.

Design of Five-transistors D-type Flip-flop Architecture

D-type Flip-flop Architecture is implemented using 45-nm CMOS technology. Schematic diagram, transient characteristics and layouts of this circuit are obtained using Cadence virtuoso simulation software. This method uses five

transistors (two PMOS and three NMOS). There are two inputs (D and Clk) and one output (OUT). The circuit diagram of the D-type Flip-flop Architecture using 45-nm design is shown in Figure 8. The dimensions of the transistors are as follows.

NMOS transistors: W = 120 nm, L= 45 nm
PMOS transistors: W = 120 nm, L= 45 nm

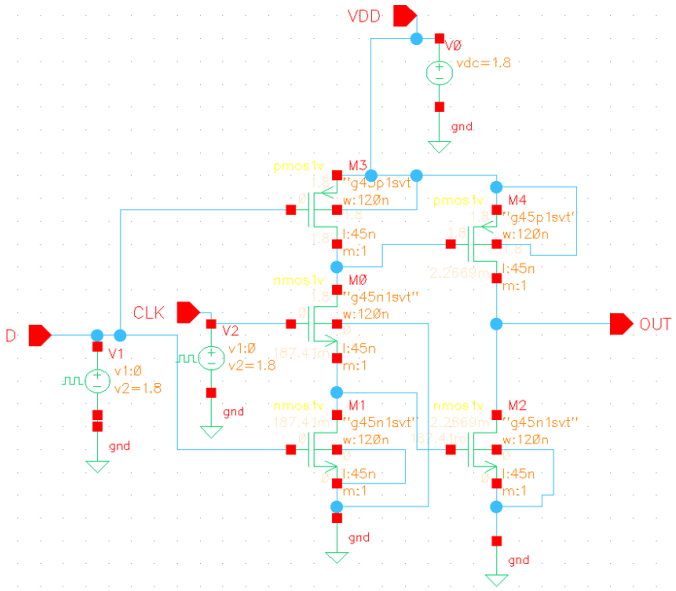


Figure 8. Circuit representation of the DFF-F Technique

Functional description of the proposed DFF-T technique

All of the D-type Flip-flop Architecture using 45-nm technologies are operated with a timing duration of 10 µs and a 1.8 V power supply.

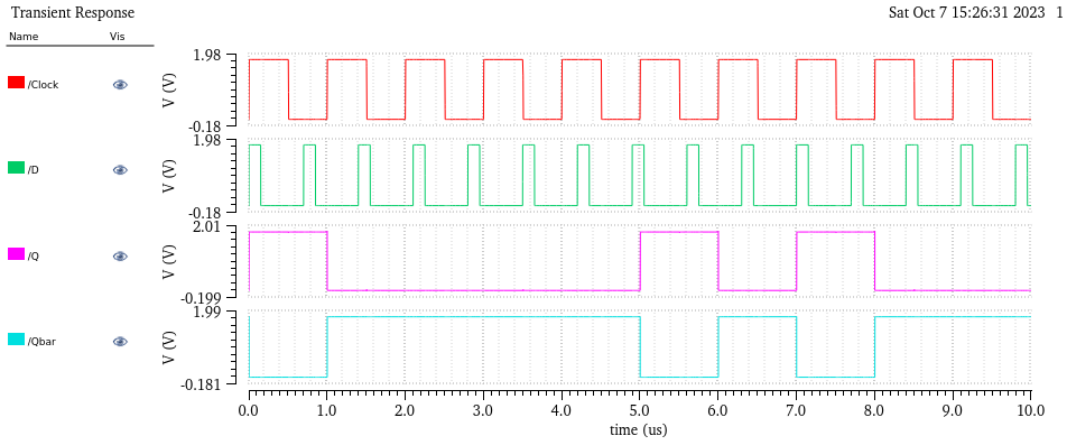


Figure 9. Transient characteristics of the DFF-T approach

. The proposed DFF-F architecture has two inputs, one for D and one for Clock, and two outputs, Q and Qbar, the complement of Q. At 1.8 V of power supply, this flip-flop functions as an edge-triggered D-type flip-flop. Using 45nm technology, Cadence's Virtuoso Tool designed this schematic. The clock signal serves as a controller for the flip-flops.When the transition of the input clock pulse changes, the D-type flip-flop changes its state in accordance with its characteristic table.

When the clock pulse of the D-type flip-flop is on the positive-going- edge, as shown in Figure 9, the output waveform changes states.

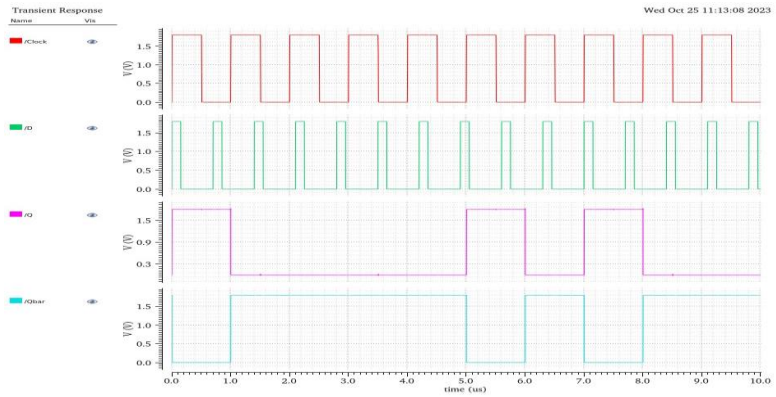


Figure 10. Transient characteristics of the DFF-DL approach

All mehods of DFF architectures have the same characteristics. Therefore, transient characteristics of the DFF-T approach is depicted in Figure 9 and transient characteristics of the DFF-DL approach is presented in Figure 10. Moreover, transient characteristics of the DFF-TG approach is depicted in Figure 11 and transient characteristics of the DFF-DL approach is presented in Figure 12.

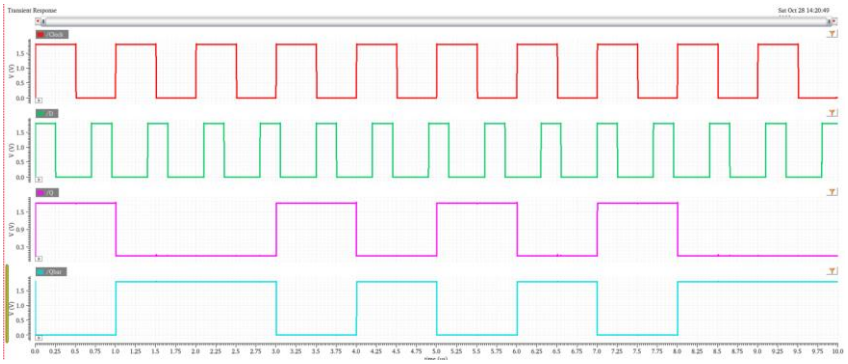


Figure 11. Transient characteristics of the DFF-TG approach

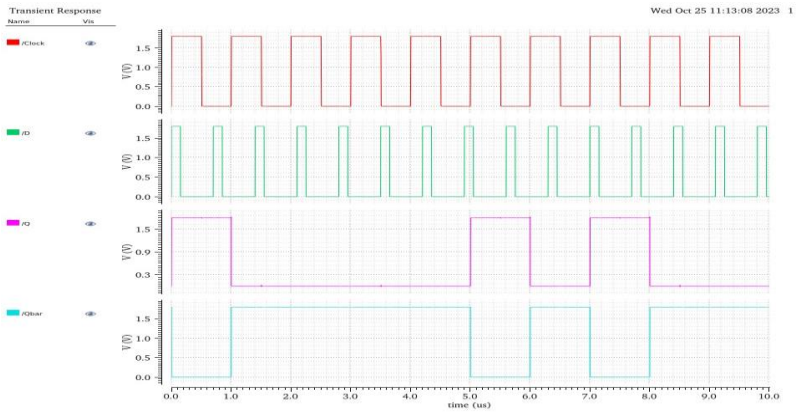


Figure 12. Transient characteristics of the DFF-F approach

Physical design methodology of the D-type flip-flops architectures

The physical designs of the D-type Flip-Flop Architecture are simulated in the Figure 13 to Figure 16 using 45-nm scaling techniques. These four circuits were designed at supply voltage of 1.8 V and 27 °C for the junction temperature.

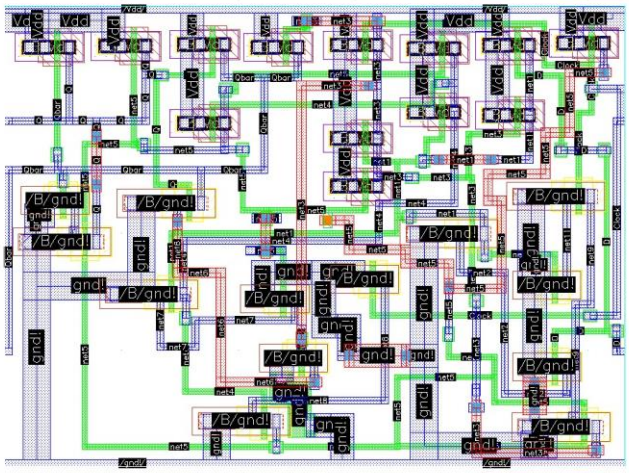


Figure 13. Layout design of the DFF-T method

The P&R boundary of the D-type Flip-Flop with Traditional techniques (DFF-T)design, which is depicted in Figure 13, is 5.31 µm × 3.945 µm (i.e. Layout area of 20.94795 µm) and has about twenty-six transistors. D-type Flip-Flop with Demorgan' s Law (DFF-DL) design has a P&R boundary of 5.385 µm × 4.81 µm (i.e. Layout area of 25.90185 µm), and has about fourteen transistors as illustrated in Figure 14.

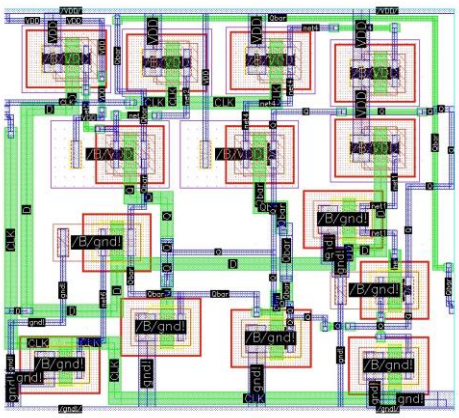


Figure 14. Layout design of the DFF-DL method

The P&R boundary of the D-type Flip-Flop with Transmission Gate (DFF-TG) design, which is depicted in Figure 15, is 4.515 µm × 2.955 µm (i.e. Layout area of 13.34 µm) and has about ten transistors. D-type Flip-Flop with Five transistors (DFF-F) design has a P&R boundary of 1.745 µm × 1.62 µm (i.e. Layout area of 2.8269 µm), as illustrated in Figure 16. To resolve any inconsistencies between the layout and the schematic, the LVS, which stands for "Layout Versus Schematic," is employed [13]. The "Design Rule Check," or DRC, is a method for verifying parameter specifications [14]. The utilization of these layouts reduces the size of

the designs, which have been verified by the DRC and LVS. In these designs, there are three metal layers that have been implemented.

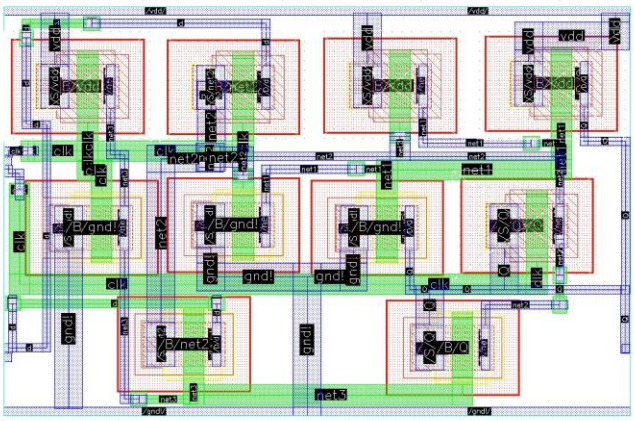


Figure 15. Layout design of the DFF-TG method

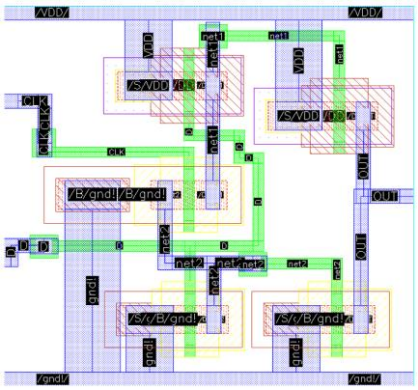
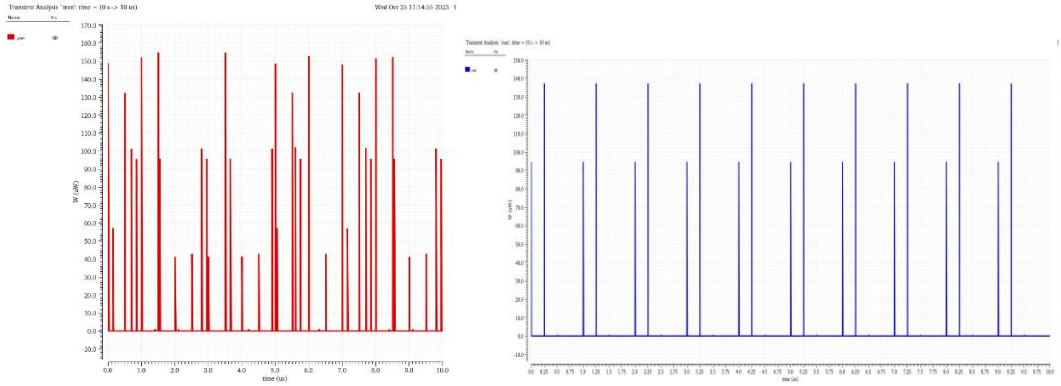


Figure 16. Layout design of the DFF-F method

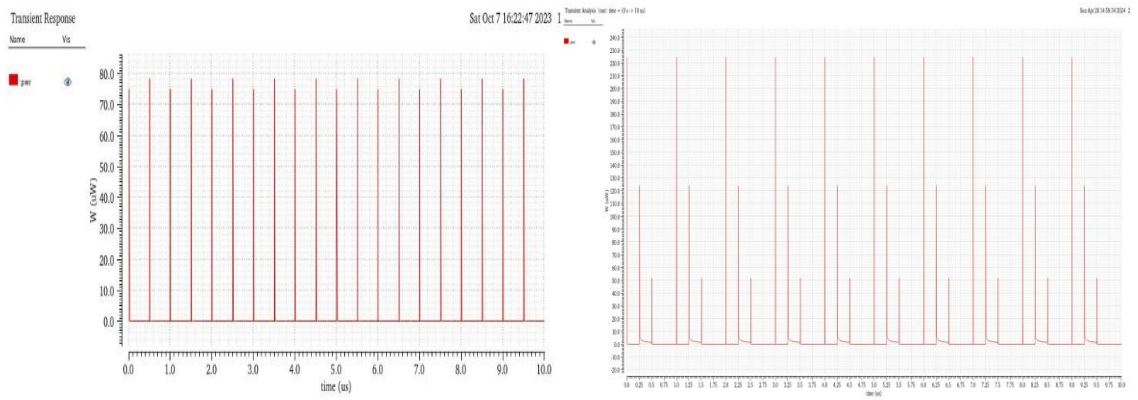
Graphs of power calculation for low-power techniques at 45 nm technology

Figures 17 (a) to (d) provide graphs of average power calculations for the power used by circuits created. As a result, the DFF-DL technique has lower power consumption when compared to other techniques. Simulation Results of power consumption are produced with analog design environment (ADE-L) simulator.



(a) (b)

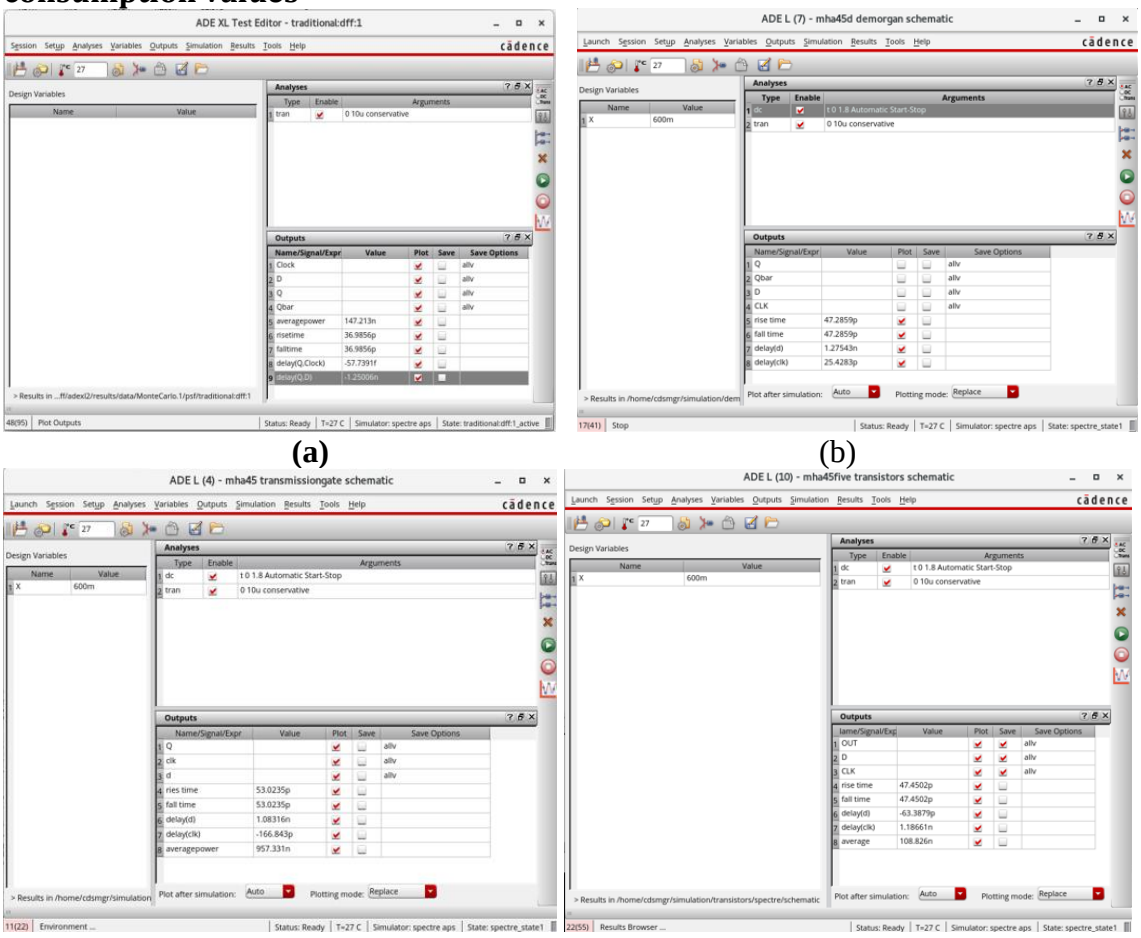
Figure 17. (a) Power consumption for the DFF-T technique,
(b) Power consumption for the DFF-DL technique,



(c) (d)

Figure 17. (c) Power consumption for the DFF-TG technique,
(d) Power consumption for the DFF-F technique,

Simulation results of Rise time, Fall time, Delay, and Average power consumption values



(a) (b)

(c) (d)

Figure 18. (a) Rise time, Fall time, Delay ,and Average power consumption values for DFF-T technique,
(b) Rise time, Fall time, Delay ,and Average power consumption values for DFF-DL technique,

(c) Rise time, Fall time, Delay ,and Average power consumption values for DFF-TG technique,

(d) Rise time, Fall time, Delay ,and Average power consumption values for DFF-F technique

Figure 18(a) to (d) shows the value of rise time, fall time, delay and average power consumption values for four methods of D-type Flip-flop architectures. These results are simulated at analog design environment (ADE-L). Figure 19 to 22 demonstrates simulation results of rise time, average power, fall time and delay by using Monte Carlo Sampling with ADE-XL simulator.

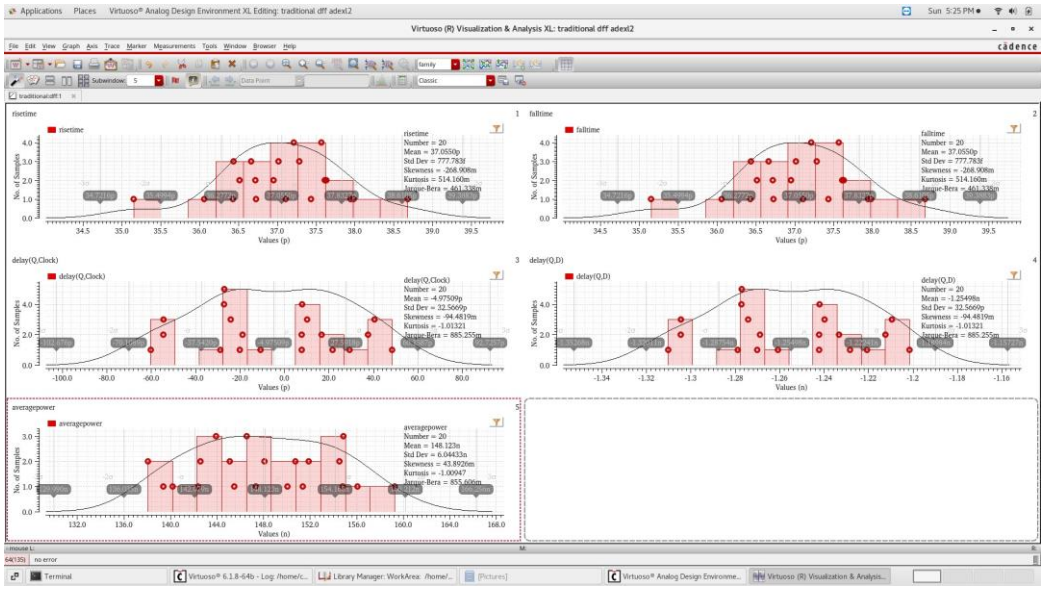


Figure 19. Simulation Results of Rise time, Fall time, Delay ,and Average power consumption for DFF-T technique by using Monte Carlo Sampling with ADE-XL simulator

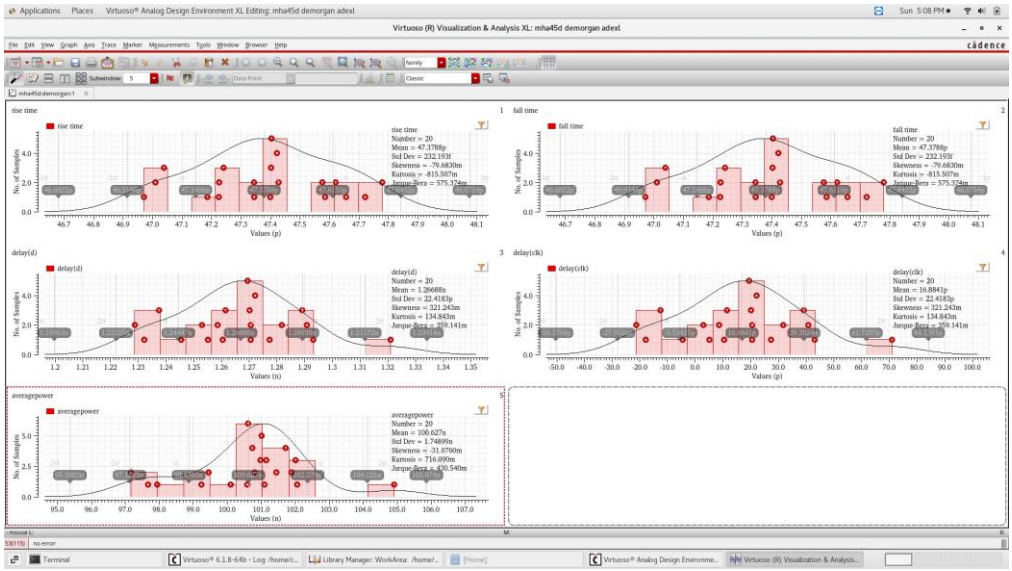


Figure 20. Simulation Results of Rise time, Fall time, Delay ,and Average power consumption for DFF-DL technique by using Monte Carlo Sampling with ADE-XL simulator

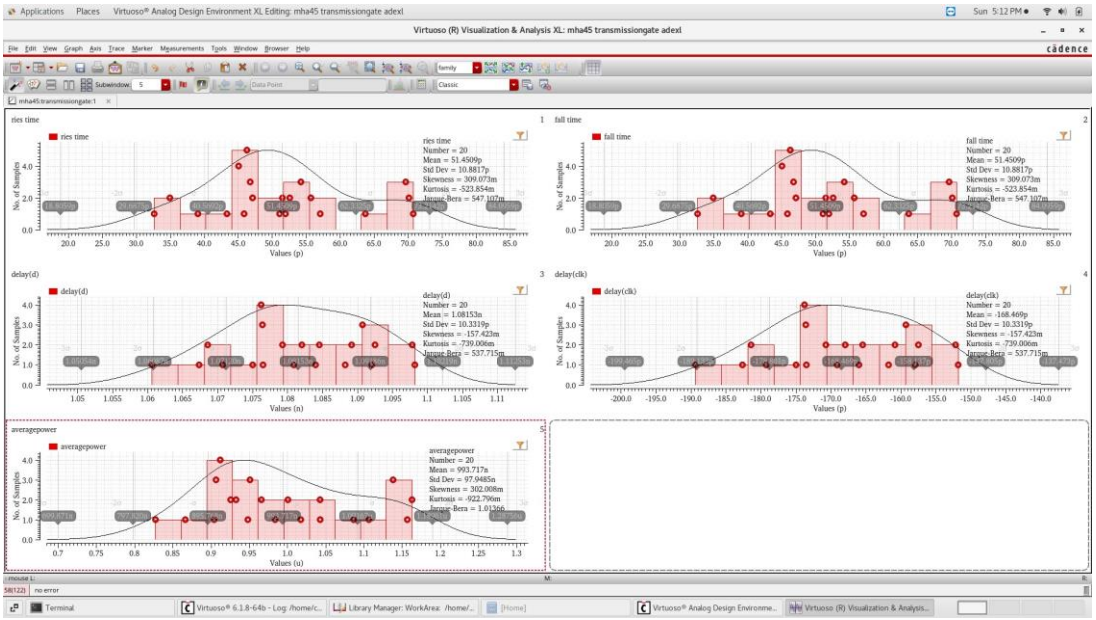


Figure 21. Simulation Results of Rise time, Fall time, Delay ,and Average power consumption for DFF-TG technique by using Monte Carlo Sampling with ADE-XL simulator

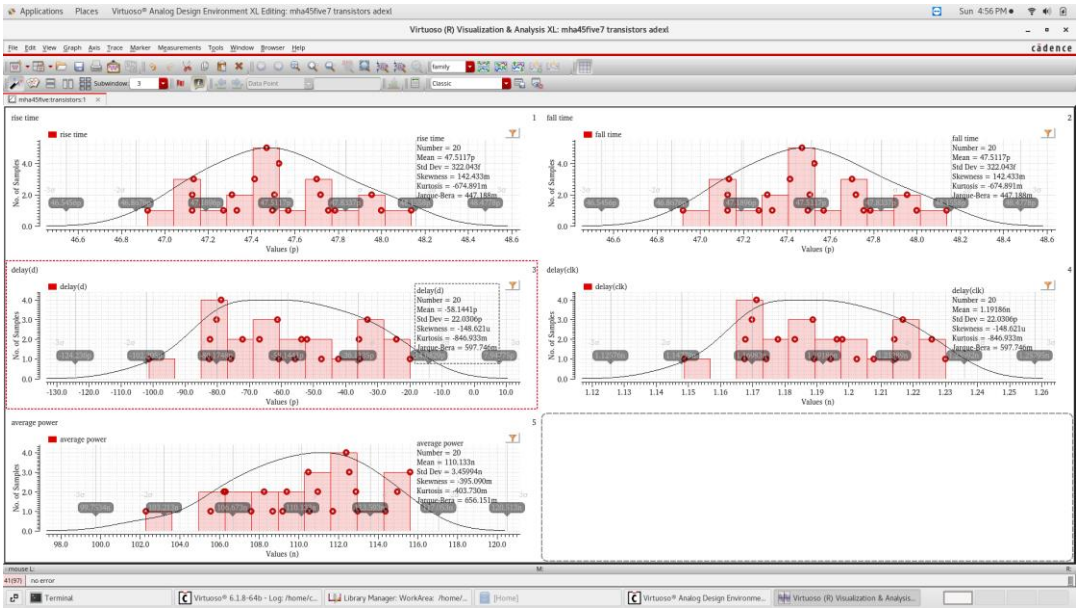


Figure 22. Simulation Results of Rise time, Fall time, Delay ,and Average power consumption for DFF-F technique by using Monte Carlo Sampling with ADE-XL simulator

Table 2 illustrate the performance comparison of different parameters in different techniques based D-type Flip-Flop (for 45nm CMOS technology). According to table 2, D-type Flip-Flop with Five Transistors (DFF-F) technique has fewer transistors count and smaller chip size when compare to the other techniques. As a result, D-type Flip-Flop with Five Transistors (DFF-F) technique has smaller production costs than the other techniques. D-type Flip-Flop with transmission gates (DFF-TG) approach yields no notable results when compared to other procedures. D-type Flip-Flop with Demorgan' s Law (DFF-DL) approach has a smallest value of average power consumption and power dissipation. D-type

Flip-Flop with Traditional techniques (DFF-T) method has a smaller value of propagation delay, rise time , and fall time. As a result, D-type Flip-Flop with Traditional techniques (DFF-T) method has a faster processing speed when compare to other techniques. Among four mehods of D-type flip-flop architecture , each method have their respective benefits.

Table 2. Performance comparison of different parameters in different techniques based D-type Flip-Flop (for 45nm CMOS technology)

Parameters	D-type Flip-Flop with Five Transistors (DFF-F)	D-type Flip-Flop with Transmission gates (DFF-TG)	D-type Flip-Flop with Demorgan' s Law (DFF-DL)	D-type Flip-Flop with Traditional techniques (DFF-T)
Transistor Count	5	10	14	26
Power dissipation	86.02 µ W	186.392 µ W	68.83 µ W	186.4933µ W
Average Power Consumption	108.826 x 10^{-9} W	957.331 x 10^{-9}W	100.4 x 10^{-9} W	147.2x 10^{-9}W
Propagation Delay (CLK-Q)	1.18661 n s	-166.843 p s	25.4283 p s	-57.739 f s
Power delay Product (CLK-Q)	1.2913 x 10^{-16} J	1.5972x 10^{-16} J	2.55x 10^{-18} J	8.499x10^{-21} J
Risetime (ps)	47.4502	53.0235	47.2859	36.9856
Falltime (ps)	47.4502	53.0235	47.2859	36.9856
Layout Length (µm)	1.745	4.515	5.385	5.31
Layout Width (µm)	1.62	2.955	4.81	3.945
Layout Area or chip size (µm^2)	2.8269	13.34	25.90185	20.94795

D. Conclusion

The 45nm CMOS technology was used to implement the schematic diagrams, transient characteristics, and layout designs of four CMOS-based D-type flip-flop architectures in a cadence virtuoso software environment. Their performance parameters, such as chip size area, transistor count, average power consumption, rise time, fall time, and propagation delay, were calculated and compared with each other. The DFF-DL method utilized in this comparison enhances the circuit's overall energy efficiency while consuming less average power than the other techniques. In addition, the DFF-F technique outperforms the other technique in terms of total circuit performance and production cost since it has a smaller chip size (layout area),and fewer transistor counts. At 45nm technology, the DFF-F approach reduces average power consumption by 40.4899% when compared to the DFF-T technique. Processing times have been reduced by the DFF-T technology because it has a lower propagation delay value, fewer rise times, fewer fall times and lower power delay product than the other technologies. This comparison shows that each of the approaches has unique benefits and capabilities that are essential electronic technologies needed for advances in science. Among these

approaches, the DFF-F technique is ideal for VLSI applications because of its diminished chip size (layout area) and cheaper manufacturing costs.

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