Indonesian Journal of Computer Science
ISSN 2549-7286 (*online*)
Jln. Khatib Sulaiman Dalam No. 1, Padang, Indonesia
Website: ijcs.stmikindonesia.ac.id | E-mail: ijcs@stmikindonesia.ac.id

Comparative Analysis of High Speed and Area Efficient Full-Adder using CMOS and MGDI Techniques

Hnin Ngwe Yee Pwint[1], Tin Tin Hla[2]
hninngweyeepwint12@gmail.com, tintinhla99@gmail.com
Department of Electronic Engineering, Mandalay Technological University, Patheingyi Township, Mandalay City, Myanmar

Article Information

Submitted : 11 May 2024
Reviewed : 15 May 2024
Accepted : 15 Jun 2024

Keywords

Full adder, CMOS, MGDI, High speed, Delay, Area efficient

Abstract

Extremely quick processing is crucial for very large-scale integrated (VLSI) circuits in the arithmetic logic unit. Complementary metal oxide semiconductor (CMOS) and modified gate diffusion input (MGDI) are beneficial technologies for designing high-speed circuits with better reliability and performance with regard to area and power consumption. This research work provides a comparative performance analysis of a full adder that is implemented with CMOS and MGDI technology. This work aims to develop a CMOS-based full-adder and a MGDI-based full-adder circuit for area-efficient and high-speed applications. First, the analysis and implementation of the XOR and NAND logic gates are designed using CMOS technology and the MGDI technique to create a full-adder design. The comparative analysis of integrated circuits in CMOS and MGDI technologies is primarily determined by the number of transistors and delay time. The full-adder is designed and analyzed using 90 nm technology, with performance characteristics evaluated using Cadence Virtuoso Tools.

A. Introduction

Integrated circuit designs are becoming more and more complicated these days. Very large-scale integrated (VLSI) is widely used in the design of electrical components containing millions of transistors, such as memory chips and microprocessors. A process known as VLSI is used to pack millions of CMOS transistors onto a single chip in order to produce a microelectronic circuit. Three key factors are speed, area, and power consumption in a VLSI design. The basic and most commonly used arithmetic function is the majority speed-limiting component of many VLSI systems; hence, increasing its speed and performance is essential. Two binary digits added together are the main function of a full-adder cell. In systems that have arithmetic logic units (ALUs), full adders are helpful. Full adders are useful in a wide range of digital electronics and circuits. The adders can be used to perform multiplication. The arithmetic and logical functions of digital systems depend on full adders. To construct integrated circuits, a variety of technologies are available, such as bipolar integrated technology, NMOS, and CMOS [1]. MGDI and CMOS technologies are used in this work. Considerations such as transistor sizing, layout optimization, power consumption, signal propagation delay, and overall circuit performance are necessary in the design of complete adders that are CMOS- and MGDI-based. The logic style that is most commonly used is standard CMOS. The main instrument used to create integrated circuits is CMOS technology. One advantage of CMOS circuits is their simple design. The entire circuit is also integrated into the chip because of its high level of integration [2-3]. GDI was presented as a potentially effective method for achieving high performance, low chip size, and less design complexity. The GDI technique's drawback is that it cannot provide the full output swing of a desired output state. Most logic operations can be carried out with the fewest transistor ranks by using the GDI approach. In comparison to the CMOS technique, the GDI technique is better suited for configuring high-speed circuit designs with fewer discrete components [4]. Related works are also described below. Kamlesh Kukreti, Prashant Kumar, Shivangi Barthwal, Amit Juyal, and Alankrita Joshi created performance analysis of full adder based on Domino logic technique. One- bit full adder circuit was optimized using CMOS based logic and domino- based logic on Cadence Virtuoso based on 0.18um technology having the supply voltage of 3V. According to estimates, the one-bit full-adder circuit based on Domino logic required 28.57% less space and introduced 47.36% less delay than the one-bit full-adder circuit based on CMOS logic [5]. Arjun Sehrawat, Vandana Khanna, Kushal Jindal designed a comparative study of CMOS logic and modified GDI technique for basic logic gates and code convertor. Using 90 nm technology, they discovered that modified GDI technique comes out to be a good substitute for existing CMOS technology that can be used in high performance and more complex digital circuits and designs [6]. Merrin Mary Solomon, Neeraj Gupta, Rashmi Gupta developed a high speed adder using GDI technique. They estimated that full adder designs in terms of area, delay and power dissipation. In addition, this design will have an improved speed and also the efficiency of the system is more compared to all the conventional techniques [7].

In this study, a full-adder is designed and examined using conventional CMOS and MGDI methods. The full-adder circuit was first constructed using a NAND and

XOR CMOS and MGDI. Adder circuits were built and analyzed using CMOS and MGDI technology at 90 nm. The propagation delay has been calculated for 90 nm technology using Cadence Virtuoso simulation. Following that, the timing waveform, power consumption, and propagation delay time of the entire design are examined. For better comprehension, the performance analysis table and graph are finally shown.

There are five sections in this paper. A general introduction to full-adder IC design is given in Section A. The modeling of the full-adder architecture and theory is covered in Section B. The CMOS and MGDI schematic is implemented in Section C. The simulation results and analysis of the system are described in Section D, while the conclusion is provided in Section E.

B. Modeling of the Full-Adder Design

CMOS and MGDI are technologies used in the fabrication of integrated circuits. It is among the most widely used technologies for constructing digital logic circuits and microprocessors. The full-adder is built with the XOR and NAND logic circuits. The modeling of the full-adder provided by the use of Quartus II software.

Full-Adder

A basic full-adder has two outputs: Sum and Cout (carry out), and three inputs A, B, and Cin (carry in). Binary numbers include sum and Cout, as indicated in Table 1. The boolean equations associated with the fundamental logic diagram for a complete full adder are shown below. Logic gates XOR and NAND are fundamental building blocks that are integrated to make a circuit that can add two binary values with a carry-in input in order to design a full adder [8]. The logic diagram of full-adder using XOR and NAND gate is depicted in Figure 1 using Quartus II software.

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + (A \oplus B).\ C_{in} \quad (2)$$

Table 1. Truth table for Full Adder

Input			Output	
A	**B**	**Cin**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

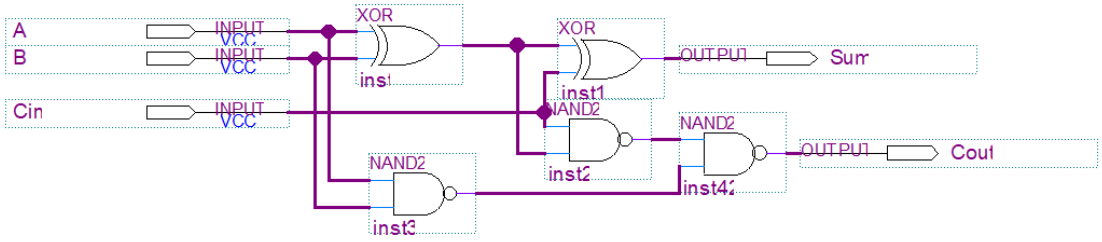


Figure 1. Logic diagram of full-adder using XOR and NAND gate

CMOS Technology

CMOS technology is a popular semiconductor technology utilized in the creation of digital integrated circuits. Particularly often used options for creating digital circuits is CMOS technology, which has various advantages over alternative technologies. The fact that CMOS circuitry operates more quickly, consumes less power, and is less susceptible to noise and process variations than other types of circuitry is just one of its numerous benefits. Figure 2 illustrates how a static CMOS gate is connected to logic "0" by an NMOS pull-down network (PDN) and logic "1" by a PMOS pull-up network (PUN). The networks are configured such that one is ON and the other is OFF for a specific input pattern [9-10].

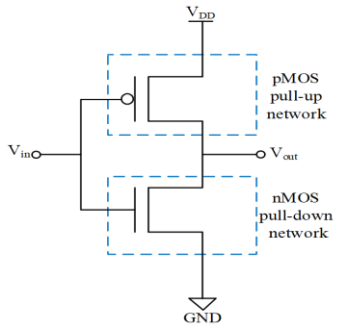


Figure 2. Logic Gate using PUN and PDN

Modified Gate Diffusion Input

In digital circuit design, gate diffusion input (GDI) is a method for effectively implementing logic operations utilizing CMOS technology. Compared to conventional CMOS implementations, GDI logic gates allow the development of complicated logic circuits with a lower transistor count. Because of this, they are incredibly effective and versatile for intricate logic systems. An improved version of the GDI technique, modified gate diffusion input (MGDI), is a high-speed and area-efficient design technique. In contrast to the basic GDI cell, where the substrate connections of NMOS and PMOS are connected to the sources of the corresponding gates, the MGDI technique connects the substrates of NMOS and PMOS to ground and VDD, respectively, and connects the gate terminal, the source of PMOS, and the source of NMOS to the input signals, as shown in Figure 3. G, P, and N are the three inputs that make up the cells in Figure 3, where G is the gate terminal and P and N are the source terminals for PMOS and NMOS. The basic GDI cell's source terminals are connected to the PMOS and NMOS substrates, while the MGDI cell's substrates are connected to ground and VDD, respectively. To obtain the intended output, connect the PMOS and NMOS drain terminals [11-12].

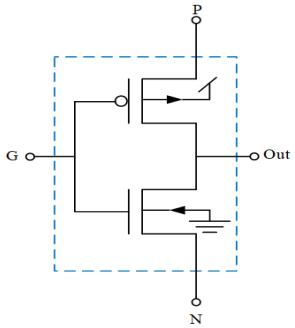
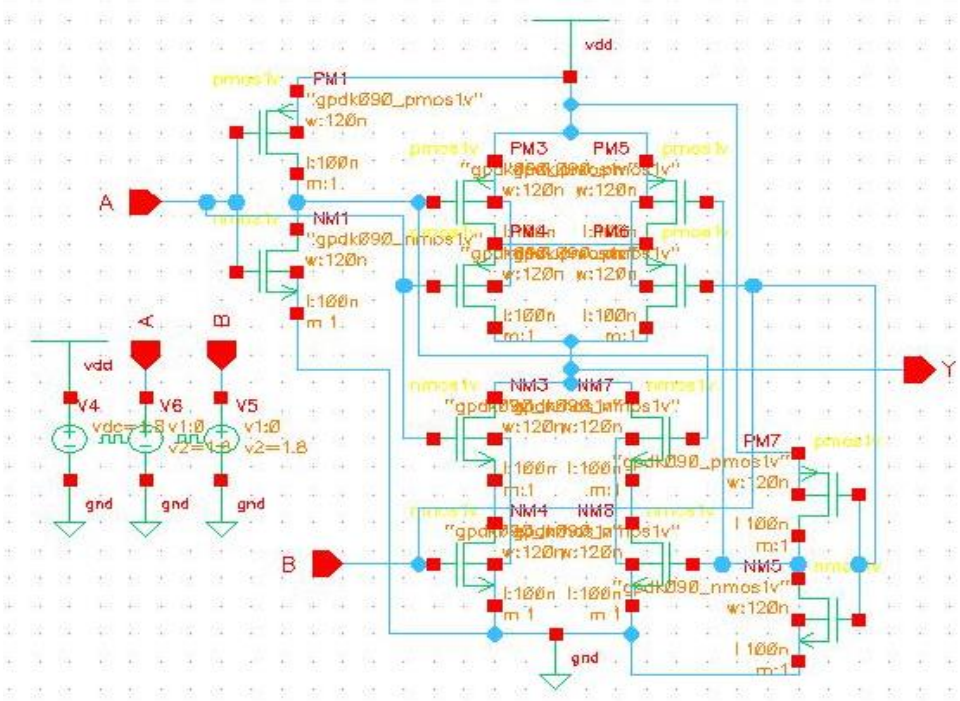


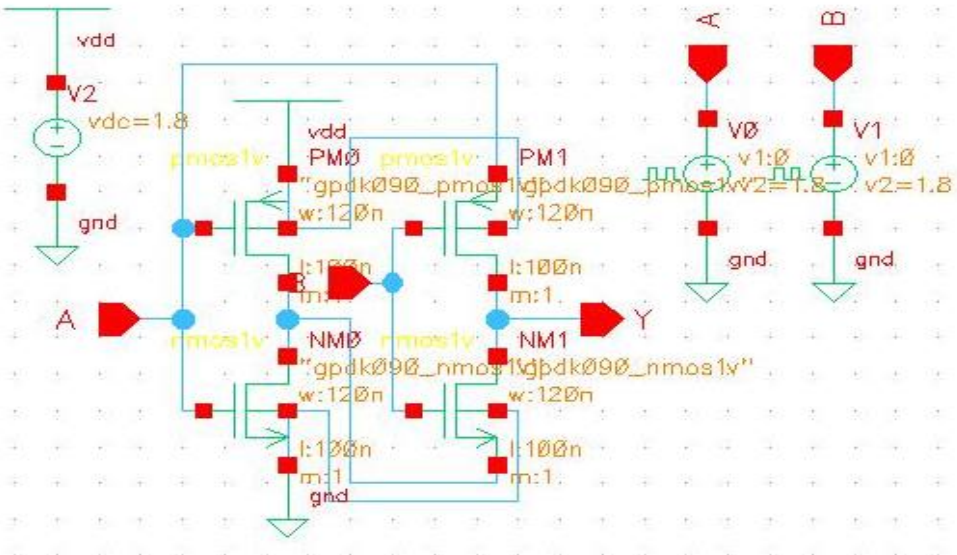
Figure 3. Modified GDI Cell

C. Creation of Full Adder Design

The schematic for a full-adder utilizing XOR and NAND CMOS-based and MGDI-based architectures is shown in Figures 4 and 5. The CMOS method was used in this design to build the XOR and NAND schematics (6 PMOS and 6 NMOS for XOR and 2 PMOS and 2 NMOS for NAND, respectively). PDN and PUN are connected by a basic structure. Additionally, the MGDI approach was used to produce the XOR and NAND schematics in design (2 PMOS and 2 NMOS for XOR and 2 PMOS and 2 NMOS for NAND, respectively). Using Cadence Virtuoso Tool's 90 nm GPDK technology, all of these schematics were created.

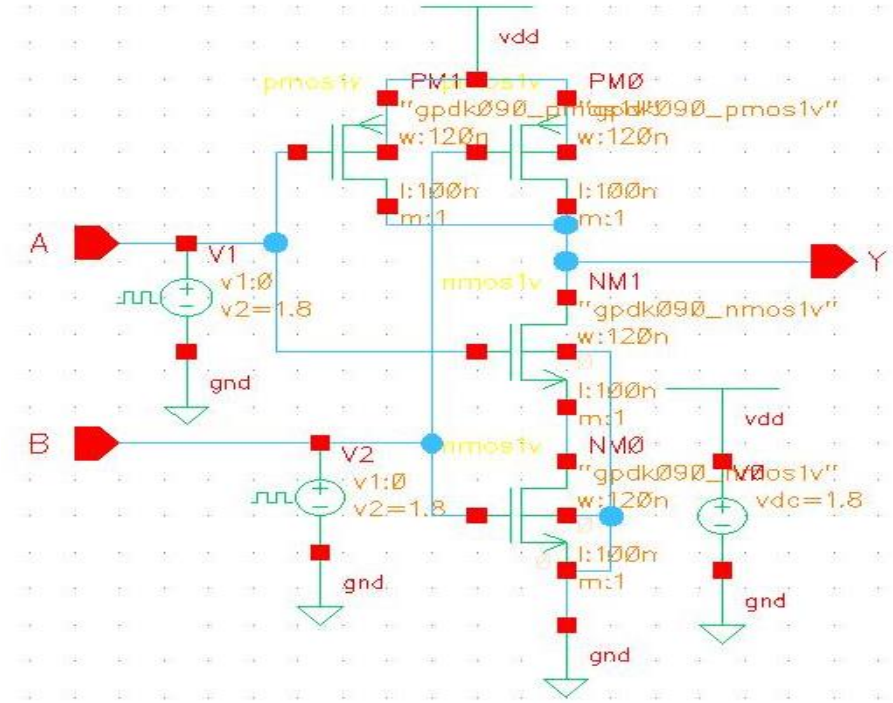


(a)

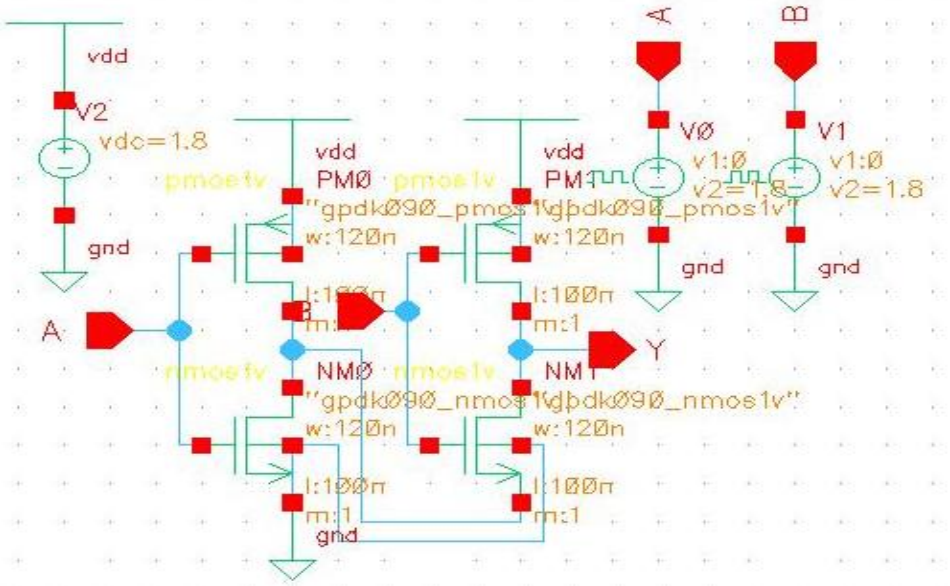


(b)

Figure 4. XOR Schematic (a) CMOS (b) MGDI



(a)



(b)

Figure 5. NAND Schematic (a) CMOS (b) MGDI

A CMOS-based full-adder schematic using 36 transistors (18 PMOS and 18 NMOS) is shown in Figure 6. Figure 7 shows an MGDI-based full-adder schematic made with 20 transistors (10 PMOS and 10 NMOS). Transistor size is expressed as a width/length (W/L) ratio. The W/L ratios of the NMOS and PMOS transistors used in all simulations are 120/100 for NMOS and 120/100 for PMOS. The Cadence Virtuoso, which operates on 90 nm GPDK technology, was used to generate this schematic.

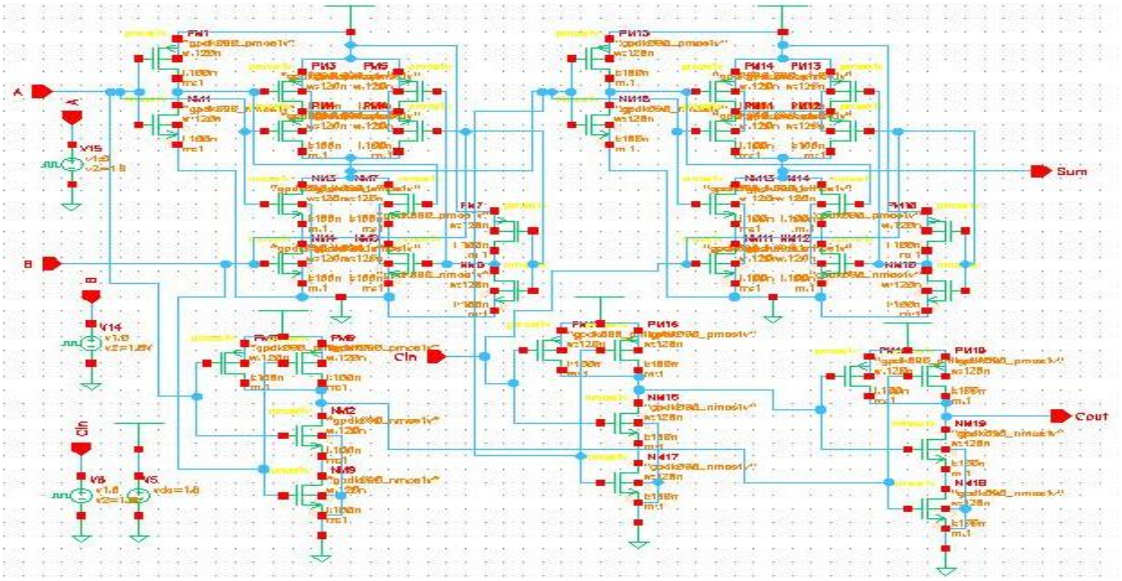


Figure 6. Full-Adder Schematic by CMOS-based

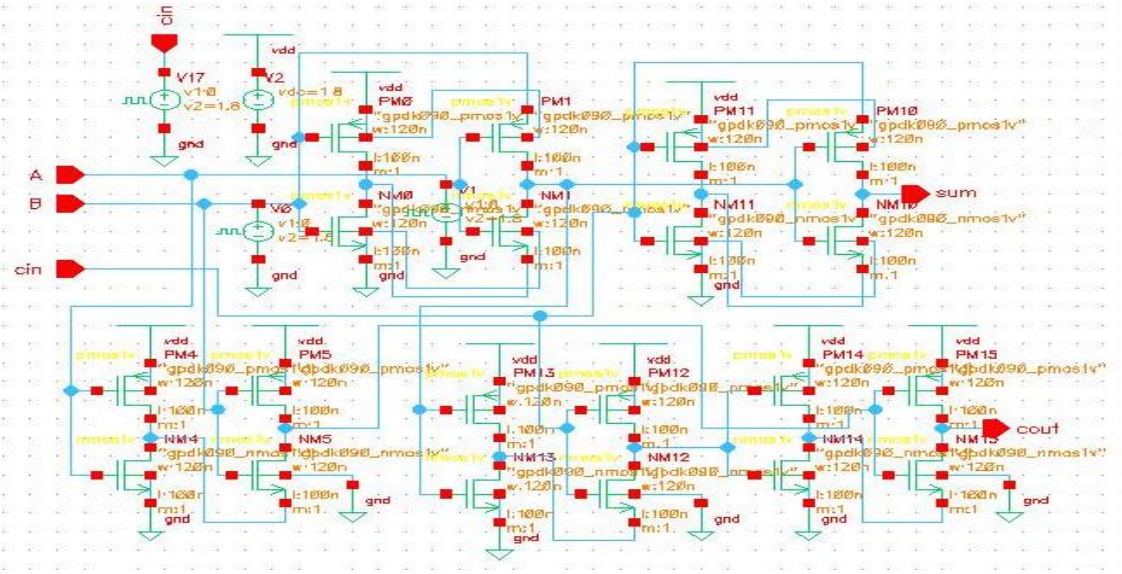


Figure 7. Full-Adder Schematic by MGDI-based

D. Result and Discussion

In this section, performance analyses of full adder designs are discussed. To validate the logic operations, schematic designs are simulated. When there are an odd number of high states in the input, the output "Sum" is high; otherwise, it is low. Similarly, when two or more input states are high, output "Cout" is high. Figures 8 and 9 displays the schematic output timing waveform. After the precise result was obtained, the power analysis waveform simulation results are shown in Figures 10 and 11 below, respectively. The waveform is also simulated with 90 nm technology at 1.8 V supply voltage, and 200 ns stop times, respectively. For all levels, the threshold voltage has been set at 0.9 volts. This voltage marks the point at which power and current start to increase as the supply voltage rises. Operating temperatures have been specified for all designs at 27°C.

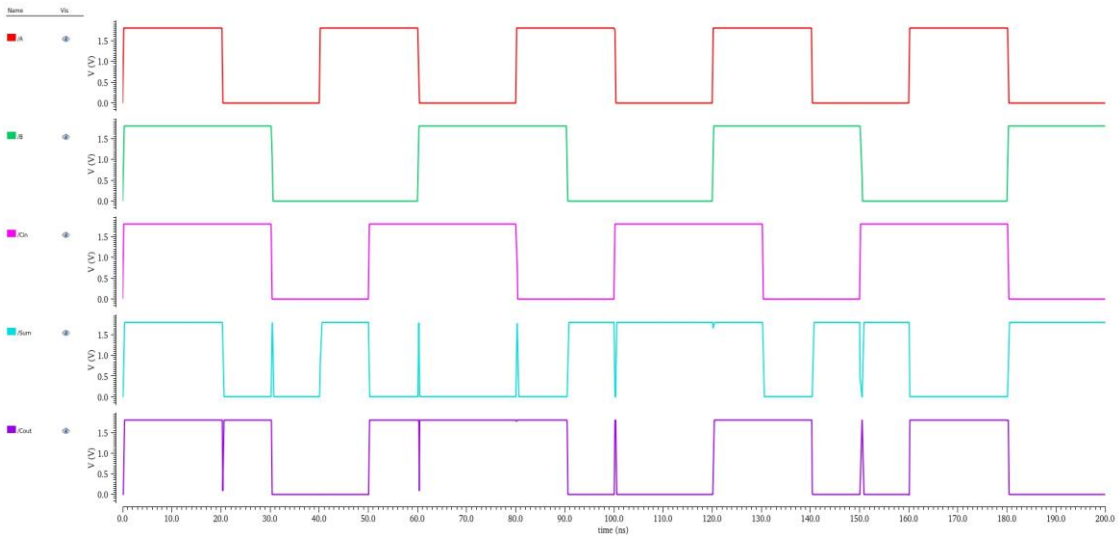


Figure 8. Full-Adder Output Timing Waveform using CMOS

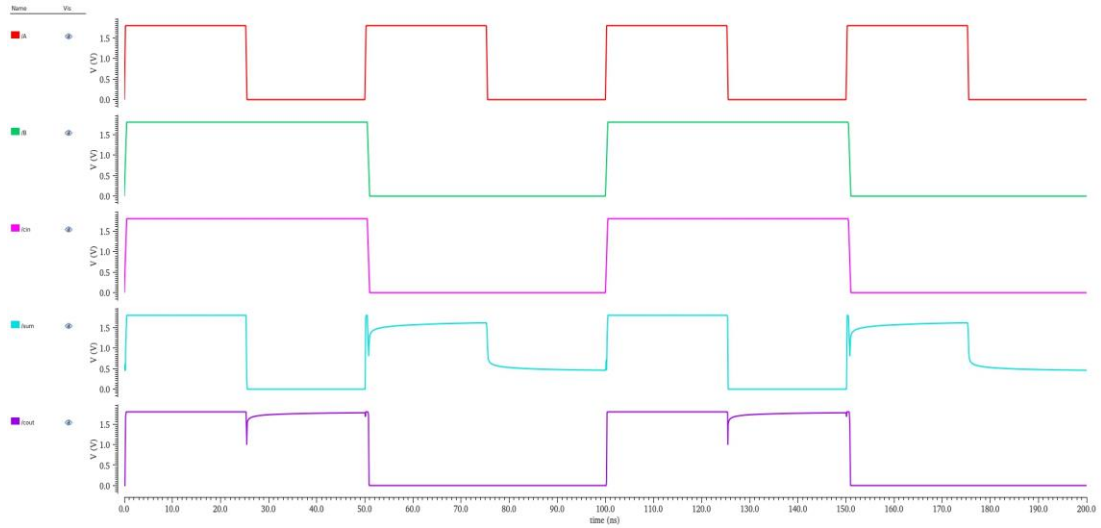


Figure 9. Full-Adder Output Timing Waveform using MGDI

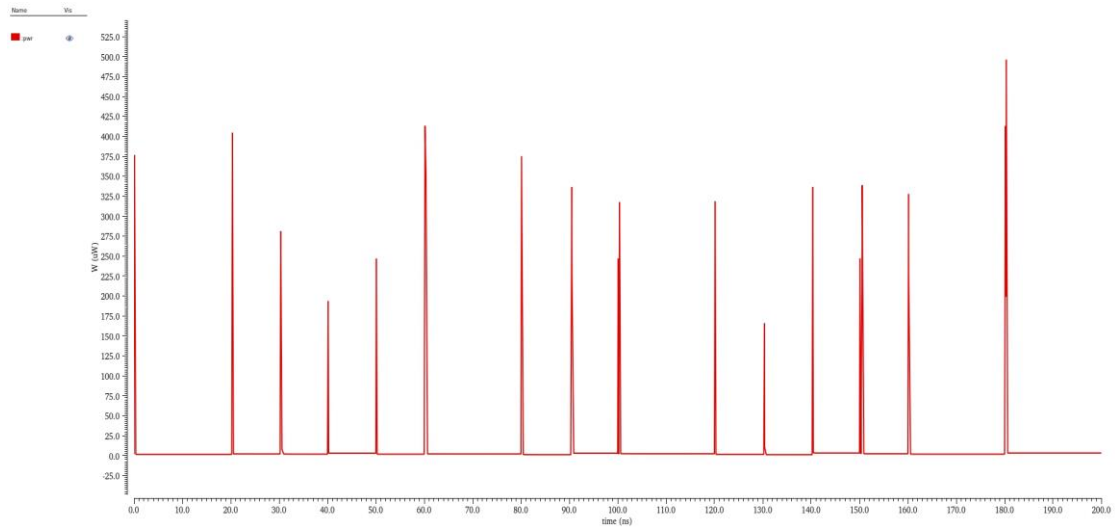


Figure 10. Average Power of Full-Adder using CMOS

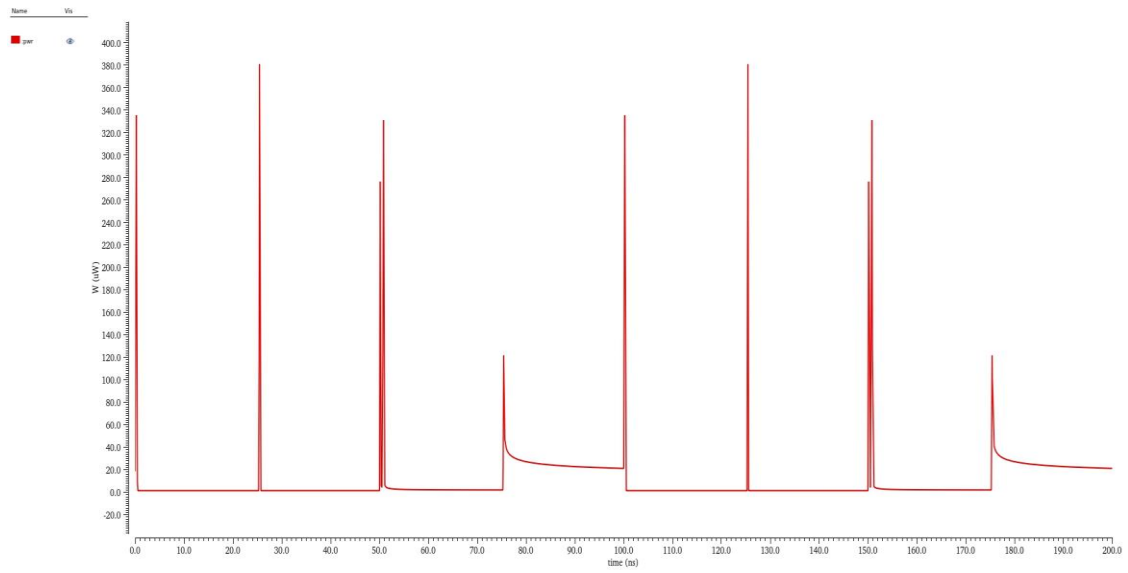
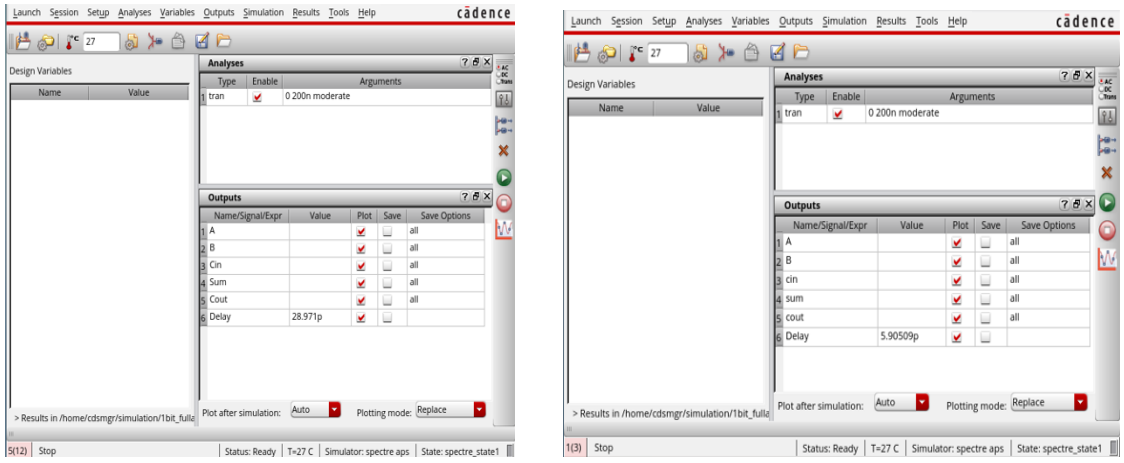


Figure 11. Average Power of Full-Adder using MGDI

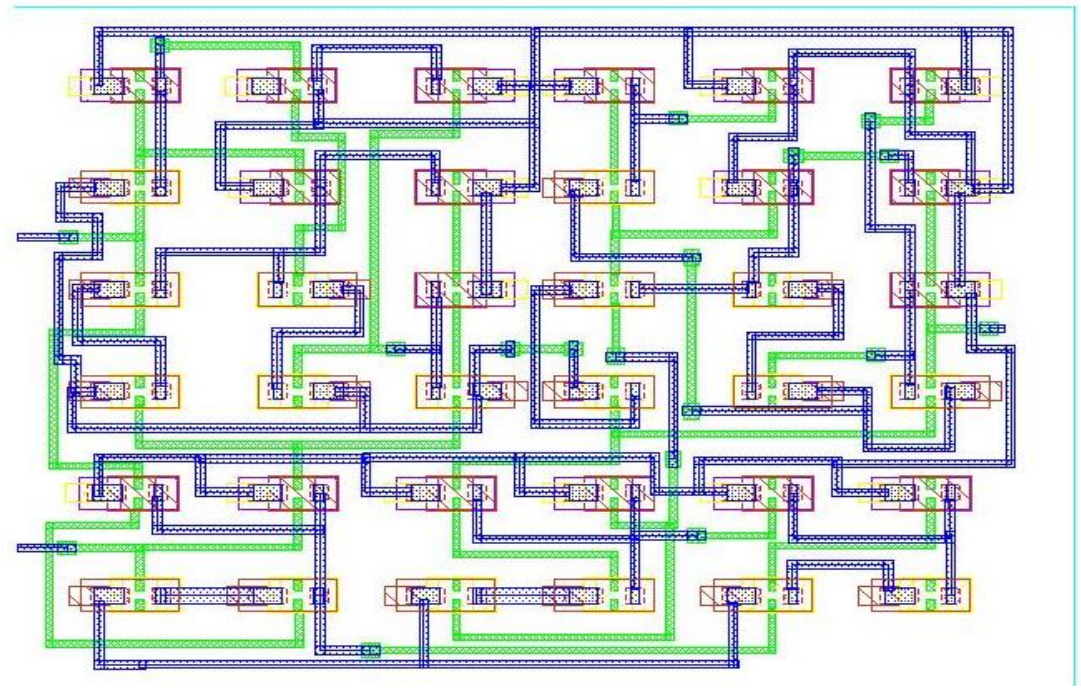
An analysis of the CMOS-based and MGDI-based full-adder circuits' delay times under input and output conditions is shown in Figure 12. The design simulation was carried out using Cadence Virtuoso in the ADE L environment. According to ADE L simulation results, the delay time results of full adder designs using 90 nm technology are 28.971 psec and 5.90509 psec, respectively. It was discovered that the delay time of the MGDI-based full-adder design is less as compared to the CMOS-based full-adder design.



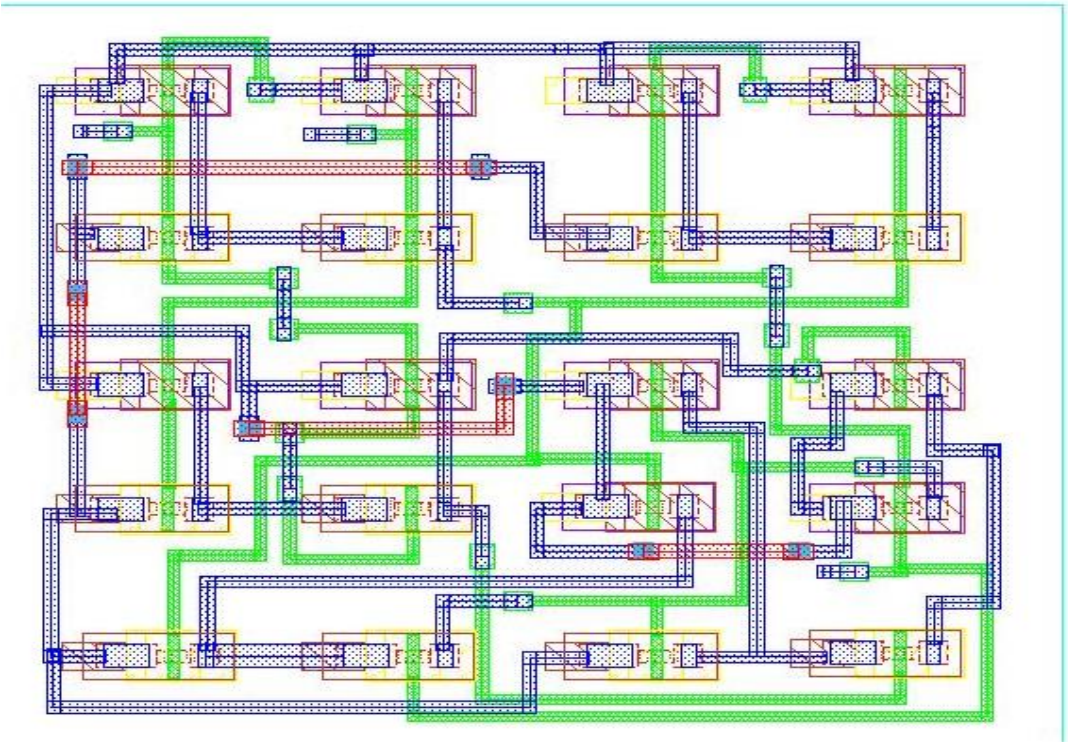
(a) (b)

Figure 12. Delay Time of Full-Adder (a) CMOS (b) MGDI

The process of producing an IC layout design involves converting the logical and schematic representations of the circuits into a physical design that can be created in a semiconductor manufacturing process. The layout designs for the CMOS-based and MGDI-based full-adder concepts are shown in Figure 13, respectively.



(a)



(b)

Figure 13. Layout design of Full-Adder (a) CMOS (b) MGDI

The comparison of CMOS-based and MGDI-based full-adder performance is shown in Table 2. For high-speed circuit design, it includes the total number of transistors, area efficiency, and delay time. The design and simulations were done with the Cadence Virtuoso. In Figure 14, the full-adder comparison analyses are shown graphically.

Table 2. Performance Evaluation of Full Adder

Full Adder Parameters	CMOS Conventional	MGDI
VDD/Vout (V)	1.8	1.8
Transistor Count	36	20
Delay (ps)	28.971	5.90509
Width (µm)	13.82	8.96
Height (µm)	10.11	7.62
Surface Area (µm²)	139.72	68.2752
Temperature (•C)	27	27
Technology (nm)	90	90

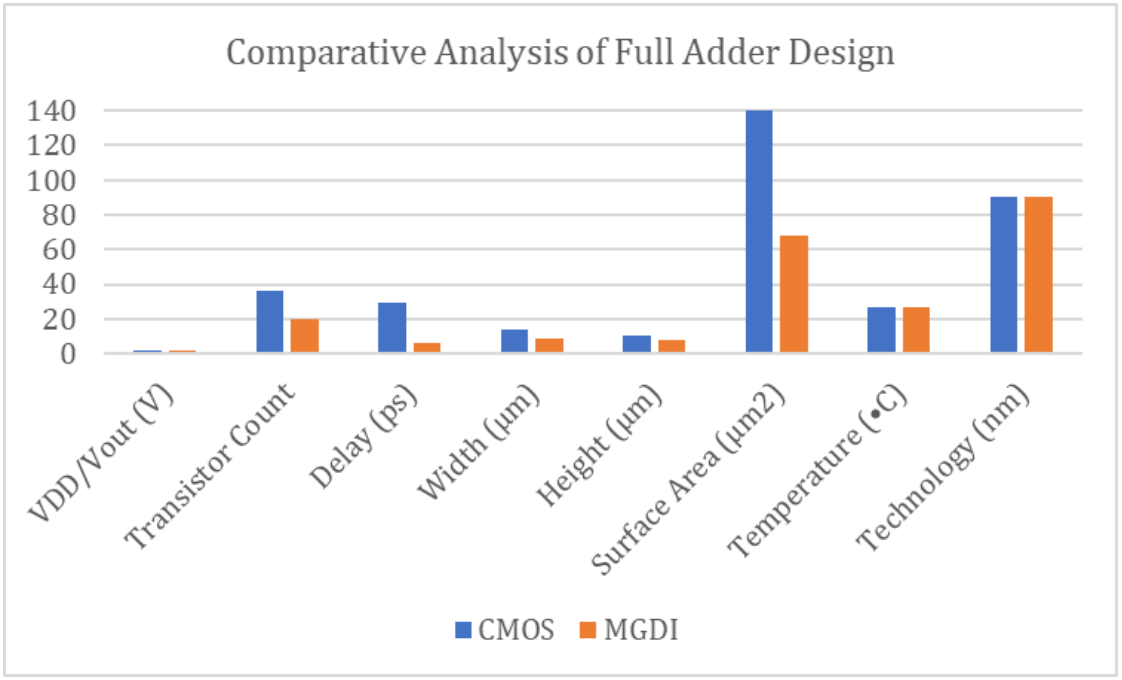


Figure 14. Full-Adder Comparative Graph

E. Conclusion

The main focus of this research work was to use CMOS and MGDI techniques to create a full adder with high-speed performance. The design of a CMOS and MGDI full-adder based on 90 nm GPDK technology at 1.8 V in Cadence Virtuoso Tool has involved a schematic analysis and comparison of surface area, transistor count, and delay. According to the simulation results, the MGDI design technique produces very accurate results with fewer transistors and less delay than the CMOS design. In addition, as compared to CMOS logic, the MGDI technology results found a 79.6172% reduction in delay and a 51.1343% reduction in chip size. So, the MGDI technique is a superior replacement for current CMOS technology in high-performance and sophisticated digital circuits and designs.

F. Acknowledgment

The author wanted to show appreciation to Dr. Tin Tin Hla, Professor and Head, Department of Electronic Engineering, Mandalay Technological University, for her help, encouragement, and kindness in writing this research.

G. References

[1] P. Sreelatha, P.K. Lakshmi, & P. R. rao, " Performance Analysis of 1-Bit Full Adder using Different Design Techniques", *2nd IEEE International Conference On Recent Trends in Electronics Information & Communication Technology (RTEICT)*, pp. 2262-2266, May 19-20, 2017.

[2] D. Thakur, & H. Patidar, "Literature Survey on Area Optimization of CMOS Full Adder Design", *ICTACT Journal On Microelectronics*, vol. 07, Issue. 04, pp. 1241-1244, January 2022.

[3] L. Kumre, "Power and Delay Analysis of One Bit Adders", *International Conference on Intelligent Sustainable Systems (ICISS)*, IEEE, 978-1-5386-1959-9/17/$31.00 ©2017.

[4] Z. Tabassum, M. Shahrin, A. Ibnat, T. Amin, "Comparative Analysis and Simulation of Different CMOS Full Adders Using Cadence in 90 nm Technology", *3rd International Conference for Convergence in Technology (I2CT)*, IEEE, 978-1-5386-4273-3/18/$31.00 ©2018.

[5] K. Kukreti, P. Kumar, S. Barthwal, A. Juyal, & A. Joshi, "Performance Analysis of Full Adder based on Domino Logic Technique," *IEEE, Sixth International Conference on Inventive Computation Technologies (ICICT)*, 978-1-7281-8501-9/21/$31.00 ©2021.

[6] A. Sehrawat, V. Khanna, & K. Jindal, "Comparative Study of CMOS Logic and Modified GDI Technique for Basic Logic Gates and Code Convertor," *International Journal of Advance Research and Innovation (IJARI)*, vol. 9, Issue 3, pp. 276-280. 2021.

[7] M. M. Solomon, N. Gupta, & R. Gupta, "High Speed Adder using GDI Technique", *International Journal of Engineering Technologies and Management Research (IJETMR)*, vol. 5, Issue 2, pp. 130-136, February 2018.

[8] K. Stella , S. Sowmiya, & V. M. Senthilkumar, "Energy Efficient Full Adders for Arithmetic Applications Based on GDI Logic", *Asian Journal of Applied Science and Technology (AJAST)*, Vol. 1, Issue. 2, Pages 36-39, March 2017.

[9] V. Haribabu, C. Malasri, O. Jyothirmai, T. Pranathi, "Design and Implementation of Ripple Carry Adder using Various CMOS Full Adder Circuits in 180nm and 130nm Technology", *International Journal for Modern Trends in Science and Technology (IJMTST)*, Vol. 06, Issue. 03, pp. 29-33, March 2020.

[10] V. Chandralekha, L. Navya, K. Sanapala, & N. Syamala, "Performance Analysis of GDI based Arithmetic Circuits", *5th International Conference on Computing Communication and Automation (ICCCA)*, IEEE, 978-1-7281-6324-6/20/$31.00 ©2020.

[11] Ms. Vishalatchi.S, Ms. Dhanam, & Dr.Ramasamy.K, "Design,Analysis and Implementation of Various Full Adder using GDI And MGDI Technique", *International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)*, Vol. 4, Special Issue. 23, pp. 87-94, December 2017.

[12] Divya Soni1, Mihir V. Shah2, "Review on Modified Gate Diffusion Input Technique", *International Research Journal of Engineering and Technology (IRJET)*, Vol. 04, Issue. 04, pp. 874-878, April 2017.