Indonesian Journal of Computer Science
ISSN 2549-7286 (*online*)
Jln. Khatib Sulaiman Dalam No. 1, Padang, Indonesia
Website: ijcs.stmikindonesia.ac.id | E-mail: ijcs@stmikindonesia.ac.id

Performance Evaluation of Physical Properties on Zinc Sulfide (ZnS)-based Field Effect Transistor

Mya Su Kyi[1], Maung Aye[2] ,Tin Tin Hla[3]
mamyasukyi.mtu@gmail.com
Department of Electronic Engineering, Mandalay Technological University, 5071, Patheingyi Township, Mandalay Region, Myanmar

Article Information

Submitted : 5 May 2024
Reviewed : 8 May 2024
Accepted : 15 Jun 2024

Keywords

Zinc Sulfide (ZnS), Field Effect Transistor, Physical Properties, Mathematical Modelling, Semiconductor Device Modelling, Device Performance

Abstract

The paper presents the performance evaluation of physical properties on Zinc Sulfide (ZnS)-based Field Effect Transistor. The most famous III-V compound-based semiconductor devices have several affected to the environment and the toxic contents are directly responded to the society. Due to the lack of technology on nontoxic compound-based semiconductor device fabrications, the novel device with II-VI compound materials are challenging issues for the environments. The specific objectives of doing research on fabrication of II-VI compound-based semiconductor devices in advanced laboratories are to emphasize the numerical modeling of the device structure and designing the FET based on ZnS material, to contribute the mathematical model for physical characteristics of the FET structure and the modification of the device structure will be easily established by using numerical simulation. The mathematical analyses on physical properties of device structure with ZnS material are confirmed and observed the several properties of electrical and electronic characteristics. The detailed implementations for ZnS-based FET devices are performed and evaluated the performance of the developed FET devices. There are two steps analyses in physical properties of ZnS-based FET devices with numerical implementation by MATLAB languages. The results observed in this study could be confirmed with the recent works from several research laboratories and the developed ZnS-based FET devices could be utilized in high performance wide band applications on switching in the power electronics and amplification purposes in modern amplifier design in real world applications.

A. Introduction

Zinc sulfide (ZnS), a naturally happening salt, is the leading source of zinc. It has two conjoint crystalline forms (polymorphs): Sphalerite ("zinc blende"), by a cubic crystal structure, is the arrangement that preponderates in nature. Wurtzite, by hexagonal crystals, is infrequent, but it can be made by heating system of sphalerite to ≈1020 ºC. ZnS is phosphorescent, which styles it useful for quite a few electronic and decorative applications. Among its prior uses were X-ray and television screens and clock and watch dials. In this stage of development of nanotechnology, ZnS recurrently arrangements the shells of semiconductor quantum dots, with cadmium selenide (CdSe) as the cores [1].

The researcher attempted to accomplish the electrical and electronic properties analyzing of the ZnS-based FET and the other semiconductor devices by applying the computer based simulation approaches and the several experimental processes in relation to the previous literature reviews. Zinc sulfide is utilized for Field Effect Transistor. Because of their highly chemically stable, low solubility, wide band gap, wide transmission range (from visible to IR region) and unique luminescent with electrical and electronic properties. ZnS has received considerable interest over the past few years in the unique nature of broadband gap semiconductors and is considered a potential next-generation high-performance electronics product. Although the perfect ZnS doping has not yet been introduced, it exhibits the greatest electrical carrier flow between oxides and is therefore used in high speed switching devices and certain electronic devices. However, the desire to use ZnS for high-performance electronic devices has not been realized to date, owing to the inherent difficulties of obtaining ZnS and achieving proper doping. Undoped ZnS has n-conductive properties, which are not clear even though some experiments and theoretical studies have been carried out. This is mainly to make p-doping difficult, which is very important for Field Effect Transistor [2].

According to the data from the earlier literature reviews, the p-type layer can select to use as ZnS material, the Mg doped ZnS can be used as n-type layer. The c-sapphire material can be chosen as a substrate layer because it is supported to achieve the high performance Field Effect Transistor which can be used in power electronics devices. In this work, based on the introduction of band-gap engineering and doping in ZnS, researcher discussed the ZnS-based FETs, comprehensively [3]. The band-gap engineering in ZnS is first discussed, which is a very important method to design to design ZnS-based FET. And then, thermal properties can be calculated based on II-VI semiconductor materials before combining the selected materials, electrical and electronic properties too. According to the result, these material can be estimated suitable or not for Field Effect Transistor. Then, the main characteristics such as V-I characteristics and C-V characteristics of the Field Effect Transistor are also determined. Besides, switching rate as function energy for Field Effect Transistor is also estimated to determine the high performance condition. Finally, physical characteristics for Field Effect Transistor are also evaluated because it is the one important point for Field Effect Transistor [4].

The rest of the paper is organized as follows. Section II presents the materials and methods for device modelling and research methodology. Section III mentions

the analyses and implementation for numerical analyses. Section IV expresses the results and discussions on the numerical analyses on developed FET structure. Finally, section V concludes the performance evaluation of this study.

B. Research Method

The main aim of this work is to improve the utilization of the semiconductor FET devices. The objectives are (i) to analyze theoretically the electrical properties of semiconductor material (ii) to evaluate the electrical properties of semiconductor materials (ZnS and Si) for JFET (high frequency) device by theoretical approaches [5] (iii) to analyze and simulate I-V characteristics curves of FET devices based on mathematical model [6-7]. Figure 1 shows the Proposed ZnS-Based FET Structure.

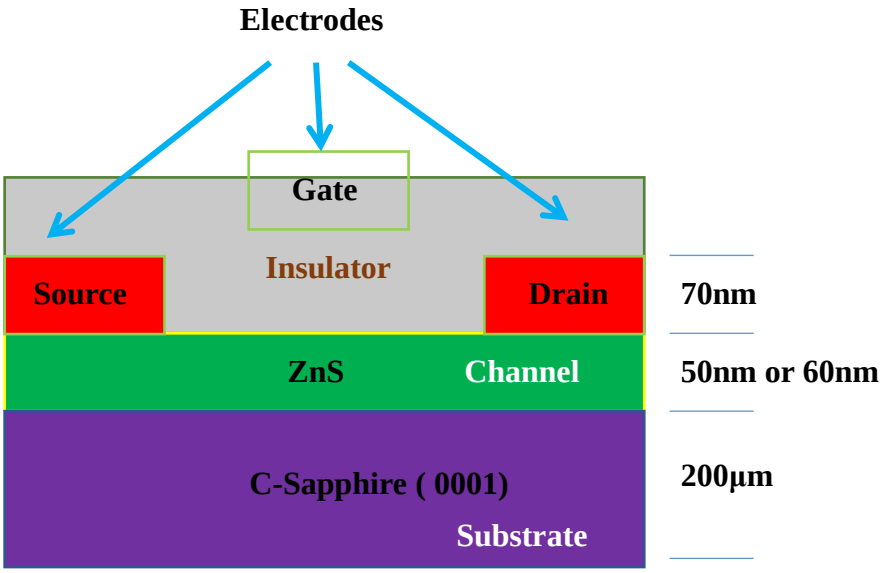

Figure 1. Proposed ZnS-Based FET Structure

Figure 2 mentions the Research Methodology. There are six steps to complete the research works. The selection of material is one of the important steps for the implementation. At present, the choice of material is ZnS for this study.

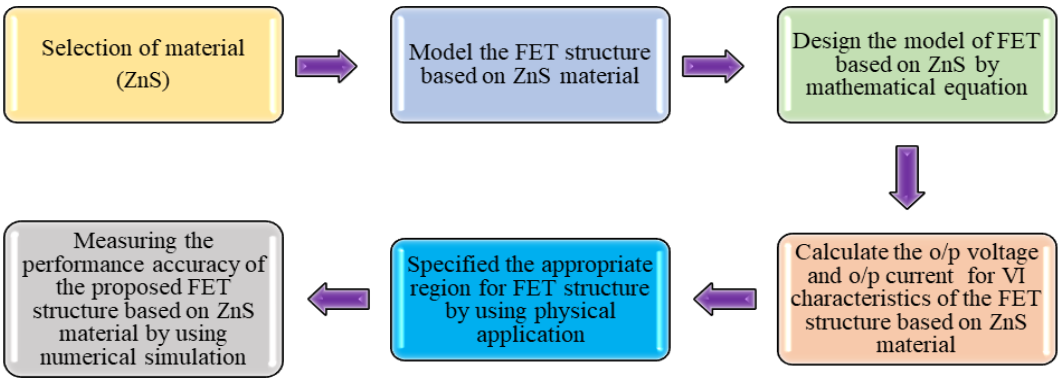

Figure 2. Research Methodology

The second step is to model the FET structure based on that materials. The next step is to design the model of the FET based on ZnS material with mathematical equations. The fourth step is to calculate the physical characteristics of FET with output voltage and output current. The next step is to specify the operating region for developed FET by physical applications. The last step is to perform the measurement results and outcomes of the results for targeted FET based on physical parameters with numerical simulation. The performance comparison was done after implementing the experimental studeis.

Analysis and Implementation

The numerical analyses and implementation for considering the physical properties of the developed ZnS-based FET structure have been accomplished by the following mathematical modelling expressions.

I_{dsat}/I_{D0} Versus V_G/V_P using the Phenomenological Relationship

It should be reemphasized that the foregoing development, and apply only below pinch-off. In fact, the competed I_D versus V_D for a given V_G actually begins to decrease if V_D values in excess of V_{Dsat}, are inadvertently substituted. As pointed out in the quantitative discussion, however, I_D is approximately constant if V_D exceeds V_{Dsat}. To first order, then, the postpinch-off portion of the characteristics can be modeled by simply setting

$$I_{D|V_D > V_{Dsat}} = I_{D|V_D = V_{Dsat}} \text{ o } I_{Dsat} \tag{1}$$

$$I_{Dsat} = \frac{2qZ\mu_n N_D a}{L}\left\{V_G - V_P - \frac{2}{3}\left(V_{bi} - V_P\right)\left[1 - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{\frac{3}{2}}\right]\right\} \tag{2}$$

The I_{Dsat} relationshtp can be simplified somewitat by noting that pinch-off at the drain end of the channel implies W→a when V(L) = V_{Dsat}. Therefore,

$$a = \left[\frac{2K_S\varepsilon_0}{qN_D}\left(V_{bi} + V_{Dsat} - V_G\right)\right]^{\frac{1}{2}} \tag{3}$$

By comparing the two eauations,

$$V_{Dsat} = V_G - V_P \tag{4}$$

V_T Versus N_A with x_0 as a Parameter (Mathematical Model)

From the qualitative description of FET operation it shunld be obvious that the parameter V_T plays a prominent role in determining the precise nature of the device charactermattes. In FET analyses V_T is commonly called the threshold or turn-on voltage. The transtutor starts to carry correct (turns on) at the onset of inversion. A compatatioeal expression for the important V_T parameter is readily established using the results and the fact that $V_G = V_T$ when $\phi_S = 2\phi_F$. Specifically, given an ideal n-channel (or p-bulk) device, simple suhsritntion yields

$$V_T = 2\phi_F + \frac{K_S}{K_O}x_o\sqrt{\frac{4qN_A}{K_S\varepsilon_o}\phi_F} \tag{5}$$

Gate Voltage Versus Surface Potential (Mathematical Model)

The gate voltage could be evaluated based on the surface potential for the confirmation of the physical properties of the FET devices.

$$V_G = \frac{kT}{q}\left[U_S + \frac{K_S x_o}{K_O L_D} F(U_S)\right] \tag{6}$$

$$L_D = \sqrt{\frac{K_S \varepsilon_o kT}{2qn_i}} \tag{7}$$

$$U_S = \frac{\phi_S}{kT/q} \tag{8}$$

P-Type Deep Depletion FET-C C-V Characteristics (Mathematical Model)

The p-type deep depletion FET-C C-V characteristics is very important parameter for analyzing the mathematical model for targeted FET device in reality.

$$C = \frac{C_O}{\sqrt{1 + \frac{V_G}{V_\delta}}} \tag{9}$$

$$V_\delta = \frac{q}{2}\frac{K_S x_o^2}{K_O^2 \varepsilon_o} N_A \tag{10}$$

$$C_O = \frac{K_O \varepsilon_o A_G}{x_o} \tag{11}$$

Depletion Width W_T Versus Acceptor and Donor Concentration (Mathematical Model)

The special note should be made of the depletion width, W_T, existing at the depletion—inversion transition point. In the delta-depletion formulation, W_T is of course the maximum attainable equilibrium depletion width. Since W= W_T when $\phi_s = 2\phi_F$ simple xuhsiitatian into W_T yields

$$W_T = \left[\frac{2K_S \varepsilon_o}{qN_A(or)N_D}\left(2\phi_F\right)\right]^{\frac{1}{2}} \tag{12}$$

V_T Versus Temperature (Mathematical Model)

The thermal voltage with respect to temperature is an outstanding parameter for designing the FET devices.

$$V_T = 2\phi_F - \frac{K_S}{K_O} x_o \sqrt{\frac{4qN_A}{K_S \varepsilon_o}\left(-\phi_F\right)} \tag{13}$$

I_D Versus V_D Characteristics with Square Law (Mathematical Model)

The output characteristics of the FET device could be evaluated based on the square law in microelectronic device theory. The following equations are very

important for designing the mathematical model of the developed FET device for real world applications.

$$I_D = \frac{Z\mu_n C_O}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right]$$

$$\begin{pmatrix} 0 \le V_D \le V_{Dsat} \\ V_G \ge V_T \end{pmatrix} \quad (14)$$

$$C_O = \frac{K_O \varepsilon_o A_G}{x_o} \quad (15)$$

I_D Versus V_D Characteristics with Physical Parameters (Mathematical Model)

The output characteristics of the FET device could be calculated based on the physical parameters in microelectronic device design. The following equations are very significant for designing the mathematical model of the technologically advanced FET device for reality applications.

$$I_D = \frac{Z\mu_n C_O}{L}\left\{(V_G - V_T)V_D - \frac{V_D^2}{2} - \frac{4}{3}V_W\phi_F\left[\left(1+\frac{V_D}{2\phi_F}\right)^{\frac{3}{2}} - \left(1+\frac{3V_D}{4\phi_F}\right)\right]\right\}$$

$$\text{for } 0 \le V_D \le V_{Dsat} \text{ and } V_G \ge V_T \quad (16)$$

$$V_W = \frac{qN_A W_T}{C_O} \quad (17)$$

I_D Ratio or Mobility Ratio Versus Temperature (Mathematical Model)

The value of drain current versus temperature is also important for checking the performance of the targeted FET device and the following equations could be utilized for optimized design structure of the FET in fabrication process.

$$\frac{g_m(T)}{g_m(300K)} = \left(\frac{\mu_n(T)}{\mu_n(300K)}\right)\left(\frac{1-\sqrt{\frac{V_{bi}(T)}{(V_{bi}-V_P)}}}{1-\sqrt{\frac{V_{bi}(300K)}{(V_{bi}-V_P)}}}\right) \quad (18)$$

$$I_D = \frac{g_m(\text{ratio})}{1+g_m(\text{ratio})R_S}V_G \quad (19)$$

C. Results and Discussions

The proposed model of ZnS FET is given in this study. The result for I_{dsat}/I_{D0} Versus V_G/V_P using the Phenomenological Relationship is also initially analyzed to observe the electrical characteristics. And also, the Linear Region for ZnS FET is also mentioned for the electrical characteristics. The Relationship of I_D Vs V_{DS} and the Relationship of I_D Vs V_{DS} are also analyzed to support to find the electrical characteristics of proposed ZnS FET. The consideration of V_T Versus N_A with x_0 as a Parameter is the main idea for observing the acceptor concentration with junction

width for optimum design of ZnS FET. The Gate Voltage Versus Surface Potential result also points out the physical characteristic could depend upon the device structure modelling in high performance condition. The p-Type Deep Depletion FET-C C-V Characteristics is the main idea for junction capacitance variations could be achieved with different voltage level for acquiring the physical characteristics. The results on V_T Versus Temperature and Depletion Width W_T Versus Acceptor and Donor Concentration highlight the confirmation of theoretical results shall have to be matched with analyses on physical parameters. The I_D Versus V_D Characteristics with Square Law and normal physical parameters could be found the checking of the optimal characteristics of the ZnS FET. The I_D Ratio or Mobility Ratio Versus Temperature directly supports the optimum value of the voltage and current relationship characteristics of ZnS FET.

The value of I_{dsat}/I_{D0} versus V_G/V_P using the Phenomenological Relationship is shown in Fig.3. The variation of I_{dsat}/I_{D0} depends on the value of V_G/V_P. Given the difference in functional forms, the agreement is quite good. This result could be support to observe the electrical properties of the proposed FET design.

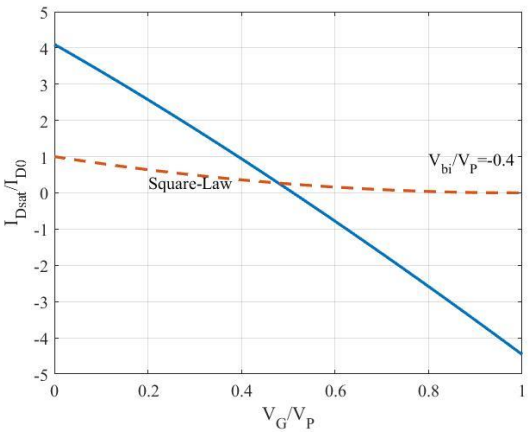

Figure 3. I_{dsat}/I_{D0} Versus V_G/V_P using the Phenomenological Relationship

The linear region for ZnS FET is given in Fig.4. The i_D is increased when the v_{DS} is also increased. The various values of i_D of i_{D1}, i_{D2}, i_{D3}, and i_{D4} could be observed with respect to different values of v_D. This results could also support to calculate the electrical characteristics of FET. The values of V_{DS} are 1.5,2,2.5,3.3.5V.

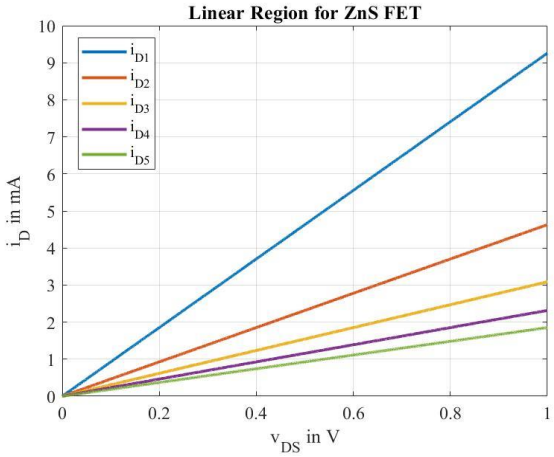

Figure 4. Linear Region for ZnS FET

The Relationship of I_D Vs V_{DS} is given in Fig.5. The values of i_D and $i_{D\ ideal}$ and V_{GS} and $V_{GS\ ideal}$ are increased when the V_{GS} is also increased. This results could also support to calculate the electrical characteristics of FET.

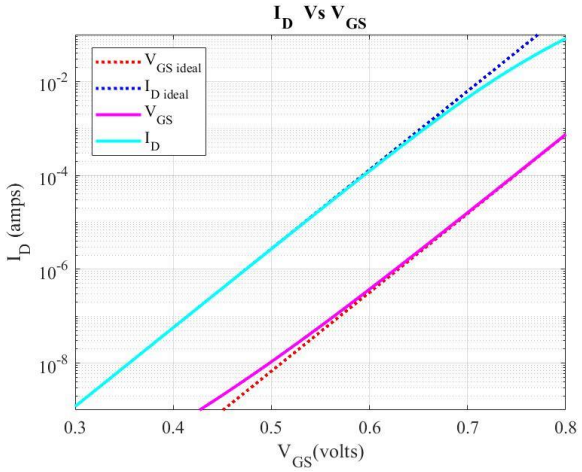

Figure 5. Relationship of ID Vs VGS

The relationship of I_D Vs V_{GS} is given in Fig.6. The V_{GS} can be changed some value in high or some value in low when the I_D is also changed. This results could also support to calculate the electrical characteristics of FET.

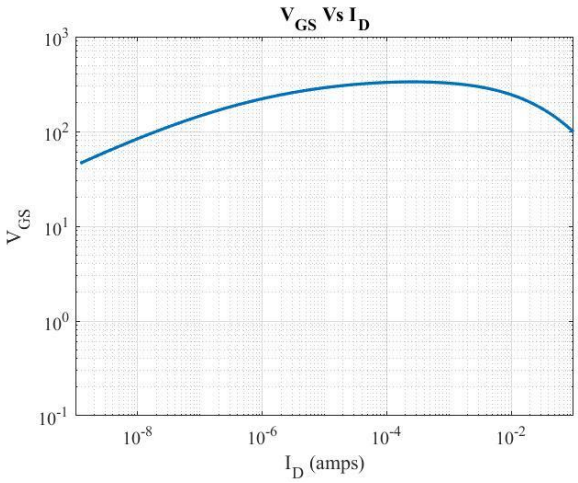

Figure 6. Relationship of ID Vs VGS

The relationship of V_T Vs N_A with x_0 is given in Fig.7. The V_T can be changed all values in high when the N_A is also increased with the decreasing value of x_0. This results could also support to calculate the voltage and current relationship characteristics of ZnS FET.

The relationship of VG Vs US is given in Fig.8. The VG shall increase when the surface potential US is also increased. Due to the variation of the surface potential for semiconductor junction, the gate voltage could be robustness of the device performance. This results could also support to calculate the voltage and current relationship characteristics of ZnS FET.

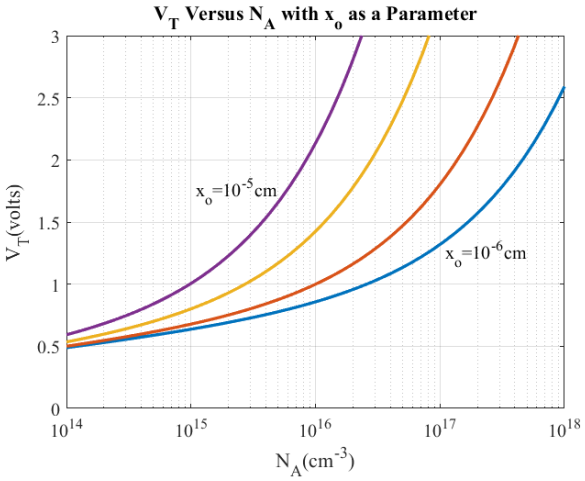

Figure 7. V_T Versus N_A with x_0 as a Parameter

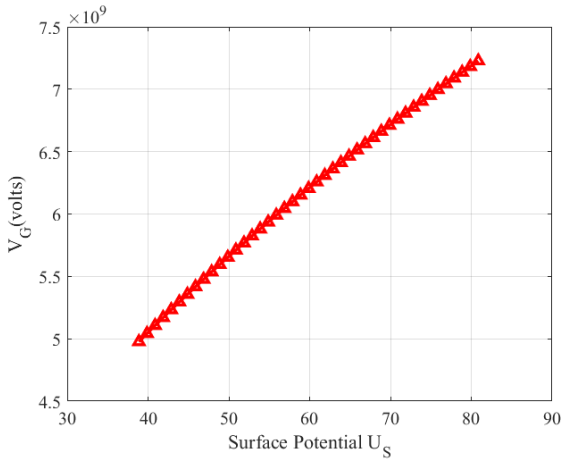

Figure 8. Gate Voltage Versus Surface Potential

The p-type Deep Depletion FET-C C-V Characteristics is given in Fig.9. The ratio of C/C_0 can decreased when the variation of V_G is also changed. The theoretical results confirmed that the device structure modelling with physical parameters of ZnS FET. This results could also support to calculate the voltage and current relationship characteristics of ZnS FET.

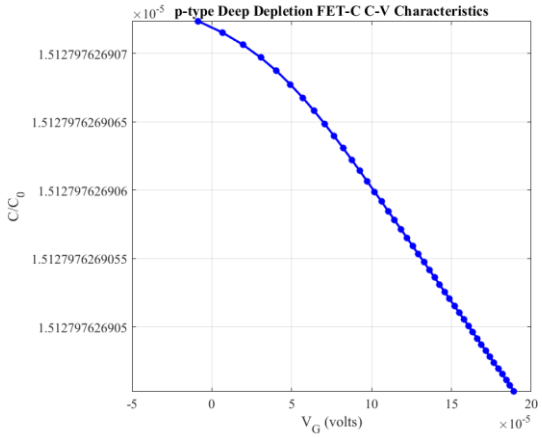

Figure 9. p-Type Deep Depletion FET-C C-V Characteristics

The relationship of Depletion Width W_T Versus Acceptor and Donor Concentration is given in Fig.10. The W_T can decreased for ZnS materials at room temperature when the N_A or N_D is also increased from 1×10^{14} to 1×10^{18} in cm^{-3}. This results could also support to calculate the voltage and current relationship characteristics of ZnS FET.

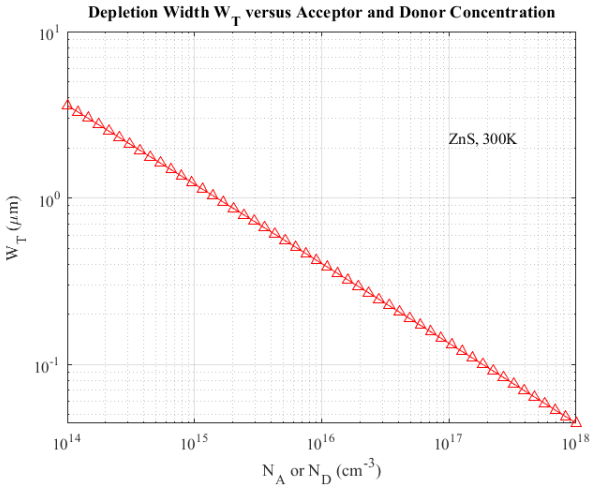

Figure 10. Depletion Width W_T Versus Acceptor and Donor

The relationship of V_T Vs Temperature is given in Fig.11. The V_T can change all value in low when the temperature is also increased. This results could also support to calculate the voltage and current relationship characteristics of ZnS FET.

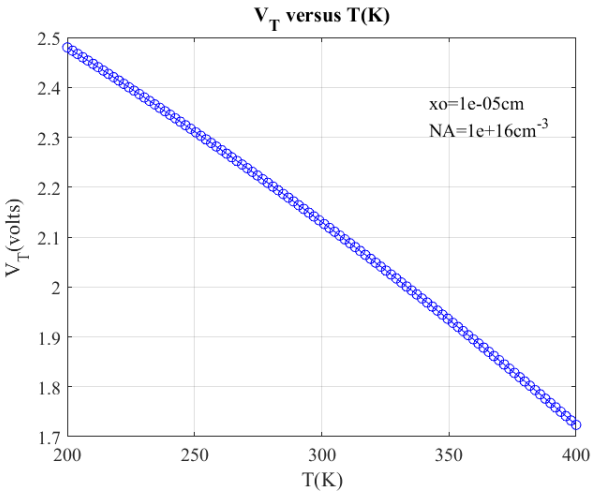

Figure 11. V_T Versus Temperature

The relationship of I_D Vs V_D is given in Fig.12. The I_D can change some value in constant for idea condition or some value in low for square law principle when the V_D is increased from 0 V to 10V. This results could also support to the optimum value calculation of the voltage and current relationship characteristics of ZnS FET.

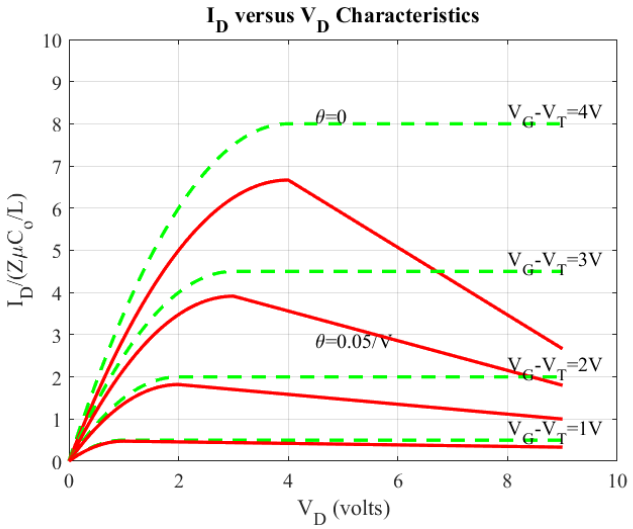

Figure 12. I_D Versus V_D Characteristics with Square Law

The relationship of I_D Vs V_D with physical parameters of ZnS FET device is given in Fig.13. The I_D can increase with constant active region from low voltage different range to high voltage different range when the V_D is also changed from 0V to 10 V. This results could also support to observe the optimum value of the voltage and current relationship characteristics of ZnS FET.

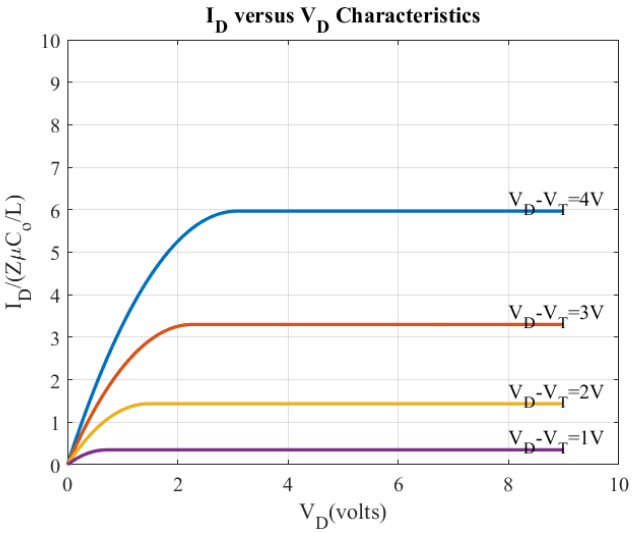

Figure 13. I_D Versus V_D Characteristics with Physical Parameters

The relationship of I_D Ratio or Mobility Ratio Versus Temperature is given in Fig.14. The I_D Ratio or Mobility Ratio can change some value in sharp low or some value in moderate low when the temperature is also increased. The room temperature point is notable for two considerations. This results could also support to observe the optimum value of the voltage and current relationship characteristics of ZnS FET.

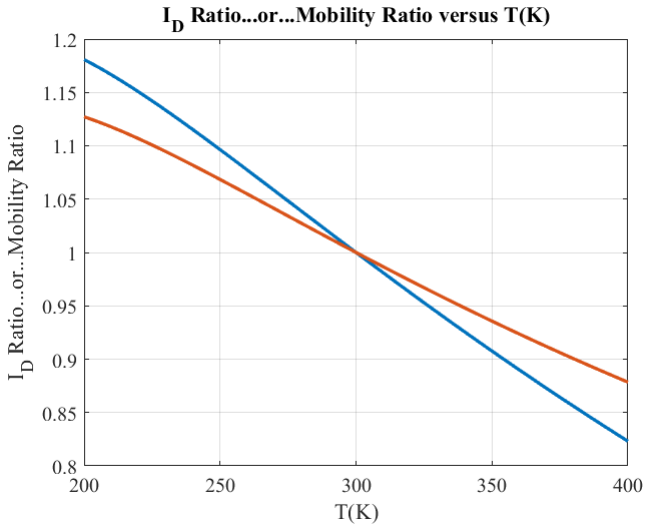

Figure 14. I_D Ratio or Mobility Ratio Versus Temperature

D. Performance Comparison

The statistics table for the performance comparison is given in Table.1. The parameters that were compared to the current research works and recent works is mentioned in that table for the confirmation of the research outcomes for the real world applications. The comparison is done with the important points for fabrication and measurement condition in experimental studies.

Table.1. Statistics Table for the Performance Comparison

	Materials Used	**Output Voltage Rate**	**Output Current Rate**	**Purposes**
[1]	Si-ZnO	Low	Low	Small Scale Devices
[2]	ZnO	Low	Medium	Medium Scale Devices
This Work	ZnS	High	High	High Performance Power Devices

E. Conclusion

This research is approached to calibrate FET design and physical characteristics of the device by applying the theoretical background. Therefore, a person who design the device may be easily applied the equations by changing the required parameters and converting the required device structure. The main method for this characterized the physical properties of field effect transistor is to use the simulation and modeling. The numerical analyses will be simulated with software tools and device characterization using mathematical modeling because of the fabrication issue in Myanmar. In this research, MATLAB programming language will be used to simulate the performance of the device.

F. Acknowledgment

The author acknowledges the semiconductor research members under the Department of Electronic Engineering of Mandalay Technological University for completing this study.

G. References

[1] Syed Zahin Reza, Md. Shahrul Islam, Fahad Al Mamun, "A Comparative Study of Electrical Properties of Si and ZnO Gate-all-around Nanowire FET", International Journal of Engineering Inventions (IJEI), Volume (6), Issue (2), PP: 58-66, Feb, 2017.

[2] Iacopi, F., Van Hove, M., Charles, M. et al. Power electronics with wide bandgap materials: Toward greener, more efficient technologies. MRS Bulletin 40, 390–395 (2015). https://doi.org/10.1557/mrs.2015.71.

[3] Douglas Henrique Vieira, Gabriel Leonardo Nogueira, Rogério Miranda Morais, Lucas Fugikawa-Santos, Keli Fabiana Seidel, Neri Alves, ZnO-based electrolyte-gated transistor (EGT) applied as multiparametric UV-sensing device, Sensors and Actuators A: Physical, Volume 347, 2022, 113989, ISSN 0924-4247, https://doi.org/10.1016/j.sna.2022.113989.

[4] Tun, H. M. ., Wulansari, R. E., Pradhan, D., & Naing, Z. M. (2023). Design, fabrication and measurement of metal-semiconductor field effect transistor based on zinc oxide material. Journal of Engineering Researcher and Lecturer, 2(3), 104–111. https://doi.org/10.58712/jerel.v2i3.103

[5] Michael S. Arnold, Phaedon Avouris, Zheng Wei Pan, and Zhong L. Wang The Journal of Physical Chemistry B 2003 107 (3), 659-663 DOI: 10.1021/jp0271054

[6] Tin Swe, H. M., Ei Khin, E., Soe, K. T., Win, L. L. Y., Tun, H. M., & Pradhan, D. (2024). Analysis of Third-Generation Solar Cell Design with Physics of Semiconductor. Journal of Novel Engineering Science and Technology, 3(02), 31–37. https://doi.org/10.56741/jnest.v3i02.525

[7] Wah, T. N., Win, T., Win, L. L. Y., Hla Myo Tun, & Pradhan, D. (2024). Analysis of Physics of Novel Light-Emitting Diode for Holographic Imaging. Journal of Novel Engineering Science and Technology, 3(02), 46–53. https://doi.org/10.56741/jnest.v3i02.566