Indonesian Journal of Computer Science
ISSN 2549-7286 (*online*)
Jln. Khatib Sulaiman Dalam No. 1, Padang, Indonesia
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Minimizing Total Harmonic Distortion of 7-Level Packed U-Cell Multilevel Inverter Using Whale Optimization Algorithm

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Article Information

Submitted : 6 Nov 2023
Reviewed: 22 Nov 2023
Accepted : 10 Dec 2023

Keywords

MLI, THD analysis, whale optimization algorithm, PUC multilevel inverter

Abstract

This paper presents an innovative study introducing a novel design for a single-phase, 7-level inverter. The design combines the modified pulse width modulation (MPWM) technique with the compact packed U-cell (PUC) topology. We evaluate this inverter's performance through comprehensive simulations in the MATLAB Simulink software. Multi-level inverter (MLI) technology is crucial for high-power, medium-voltage energy control. However, using numerous semiconductor switches in traditional MLI setups poses challenges at higher voltage levels, including increased size, costs, and losses. To address these issues, our study proposes a transformative approach, emphasizing reducing active switches within the multi-level inverter architecture. Consequently, we introduce an innovative 7-level PUC-MLI design. This configuration not only reduces harmonic distortion but also addresses cost concerns. Strategically manipulating semiconductor switch sequences significantly enhances the inverter's operational efficiency. A notable contribution is our inventive method to reduce total harmonic distortion (THD) in the inverter's output voltage, achieved through a whale optimization algorithm (WOA). Implementing this algorithm substantially lowers THD levels. Importantly, this approach's effectiveness extends to various inverter topologies and levels, offering a substantial THD reduction without additional expenses.

A. Introduction

Inverter devices play a crucial role by transforming DC into AC, a conversion process highly relevant when DC sources power AC-based consumers. While conventional four-switch H-bridge inverters are widely known, the ascent of MLI is driven by their distinctive advantages, including cost reduction, enhanced performance, and THD. Achieving efficient modulation techniques is pivotal not only in simplifying intricacies but also in minimizing manufacturing expenses, rendering MLI increasingly suitable for a broad spectrum of industrial applications.

Extensive research has converged on the domain of MLI, yielding significant contributions. Among these, the work of Akagi et al. [1] introduced the concept of instantaneous power theory, particularly for power conditioning. Rodriguez et al. [2] provided an encompassing survey of diverse multilevel inverter topologies, while Kouro et al. [3] delved into the recent strides made in this field along with its industrial utilities. Investigating hybrid MLI, Abu-Rub et al. [4] presented a comprehensive review. Meanwhile, the innovative MLI topology tailored for grid-connected photovoltaic systems was proposed by Li, X, and Li, Y [5]. Lai and Peng [6] provided a comprehensive overview of multilevel converters and their associated merits. Bazzi et al. [7] showcased a spectrum of MLI topologies characterized by minimized switch count. Additionally, Liu and Abu-Rub [8] comprehensively evaluated multilevel dc-dc converters, and Peng [9] introduced the concept of the z-source inverter. Notably, researchers have harnessed the potential of optimization algorithms to refine inverter-switching sequences. For instance, Davoudi and Farzanehfard [10] proposed an ingenious pulse width modulation (PWM) technique using genetic algorithms (GA). Rashedi et al. [11] introduced the gravitational search algorithm for optimization, while Salimi et al. [12] employed a hybrid firefly-genetic algorithm for multi-objective optimization. Addressing the optimization of cascaded MLI, Reddy et al [13] optimal total harmonic distortion minimization in MLI using improved whale optimization algorithm. A range of investigations has utilized different optimization algorithms to optimize switching angles within MLI. This includes [14]-[18], wherein a binary-coded GA was employed to minimize THD in a 7-level inverter. Similarly, [19] minimization of total harmonic distortions of cascaded H-bridge (CHB) MLI by utilizing bio inspired AI algorithm and comparison of GA and partical sward optimization (PSO) Optimized Switching Angles for 3-phase 15-Level Asymmetrical Multilevel Inverter in [20]. Finally, [21] Reducing THD of 7-Level packed U-cell multilevel inverter using GA.

As previously mentioned, a significant amount of research has been conducted to reduce the THD in MLI across various topologies. Researchers have employed different methods, and one novel approach involves the use of optimization algorithms for THD reduction. In our research, we applied the WOA, a metaheuristic optimizer. It is worth noting that the WOA had not been previously utilized for THD reduction in PUC-MLI, marking an innovative aspect of our research. WOA have proven their mettle in identifying optimal switching angles for multi-level inverters. In this paper, the prowess of WOA will be harnessed to optimize the switching sequence for PUC-MLI, bridging an important void in the current research landscape.

B. Research Method

a. PUC Inverter

The PUC inverter introduces a novel symmetric topology within the domain of MLIs. Its nomenclature stems from the U-shaped structure characterizing each individual unit of the inverter. The versatility of the PUC topology lies in its capacity to achieve diverse voltage levels, contingent upon the arrangement of voltage sources (typically capacitors) and switches embedded within the design [22]. The origin of this inverter traces back to its initial introduction in 2010, followed by subsequent advancements in 2015 [23].

In the context of our present investigation, our primary objective centers on the development of a 7-level single-phase inverter. This configuration is realized through the integration of six switches and two voltage sources, as elucidated in Figure 1. A pivotal merit attributed to our proposed inverter resides in its judicious utilization of semiconductor components. This judicious approach directly translates into reductions in physical footprint and overall system costs. A comprehensive juxtaposition of components employed in our proposed inverter versus alternative existing inverter topologies is delineated in Table 1, specifically under circumstances necessitating semiconductor components for generating a seven-level output voltage. The outcome, as succinctly portrayed in Table 1, unequivocally underscores the efficiency of our proposed inverter design, mandating the least number of components. For achieving the desired seven output voltage levels, the PUC topology mandates a mere 8 devices. By stark comparison, the natural point clamp (NPC) inverter necessitates 50 devices, the CHB architecture demands 15 devices, and the flying capacitor (FLC) arrangement requires 54 devices. Notably, the selection of voltage sources for our designed inverter aligns seamlessly with the equation delineated in (1), thereby facilitating an optimal and resource-conscious design approach.

$$v1 = \frac{1}{3}\, v2 \tag{1}$$

Through the application of equation (1), coupled with adjustments to the voltage levels of the sources, and modulation coefficient manipulation, the attainment of the desired effective output voltage from the inverter becomes achievable. This investigation establishes the initial amplitude of the first DC bus at (V1 = 33V), while configuring the second DC bus with an amplitude of (V2 = 11 V). Within this study, the generation of switching signals governing the inverter's switches is accomplished using the MPWM technique.

Table 1. The number of devices for different type of inverter

Components	*NPC*	*PUC*	*FLC*	*CHB*
Power Switches (IGBTs)	24	6	24	12
Capacitors (Voltage Sources)	6	2	30	3
Clamping Diodes	20	0	0	0
Total component	50	8	54	15

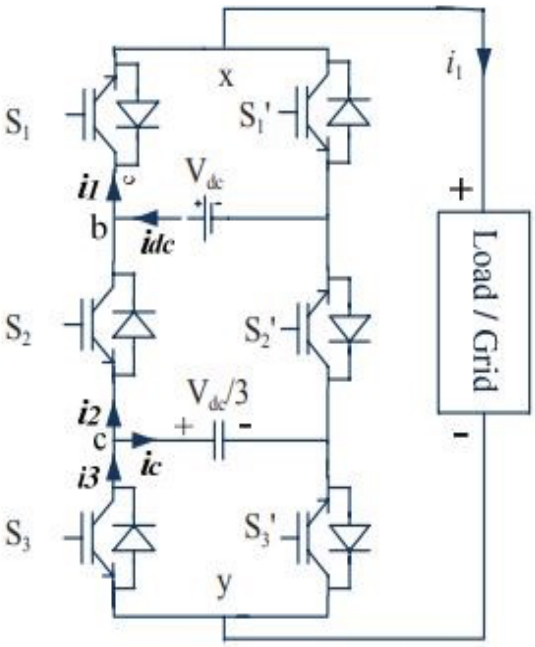


Figure 1. Schematic of A 7-level PUC-MLI with 6 switches and 2 voltage sources refers to [21]

b. Sinusoidal Pulse Width Modulation

The sinusoidal pulse width modulation (SPWM) method stands as a widely renowned approach for generating pulse signals to control an inverter's power switches. This methodology encompasses a primary reference sine wave alongside multiple triangular carrier waves. A pivotal aspect involves the comparison of the reference sine wave with these triangular carriers. In the context of this study, the SPWM technique capitalizes on six carrier waves, each contributing to the generation of pulses dedicated to the operation of the corresponding six-inverter switches. The selection of the carrier count aligns with the provisions laid out in equation (2). Notably, the determination of the carrier count is contingent upon the specific number of levels featured within the inverter configuration.

$$N = L - 1 \quad (2)$$

Equation (2) features N as the representative value for the requisite number of carriers, while L denotes the count of output voltage levels inherent to the inverter configuration. In the context of this study, the specific values employed are L = 7 and N = 6.

The design of a MLI rests upon two fundamental concepts: amplitude modulation (ma) and frequency modulation (mf). The amplitude modulation index (ma) is established as the quotient of the amplitude voltage reference signal (Vref) and the amplitude voltage carrier signal (Vcarrier), as articulated in equation (3). For the scope of this research, this ratio assumes a value of unity. Meanwhile, the frequency modulation index (mf) is defined as the ratio between the frequency

carrier signal (fcarrier) and the frequency reference signal (fref), as expressed in equation (4).

$$ma = \frac{V_{ref}}{V_{carrier}} \quad (3)$$

$$mf = \frac{f_{Carrier}}{f_{ref}} \quad (4)$$

The reference signal, in this context, takes the form of a sinusoidal wave boasting a frequency of 50 Hz and an amplitude of 3. This reference signal serves to dynamically adjust the inverter's output voltage range in accordance with shifts in the reference voltage range. The process entails the juxtaposition of the reference wave against the carrier waves, ultimately leading to the generation of switching pulses. Within the framework of this study, an amplitude modulation index (ma) of 1 is employed, emphasizing the significance of amplitude modulation. Simultaneously, the carrier frequency (fcr) is established at 1000 Hz. The schematic arrangement employed to realize seven levels of the SPWM technique is visually depicted in Figure 2.

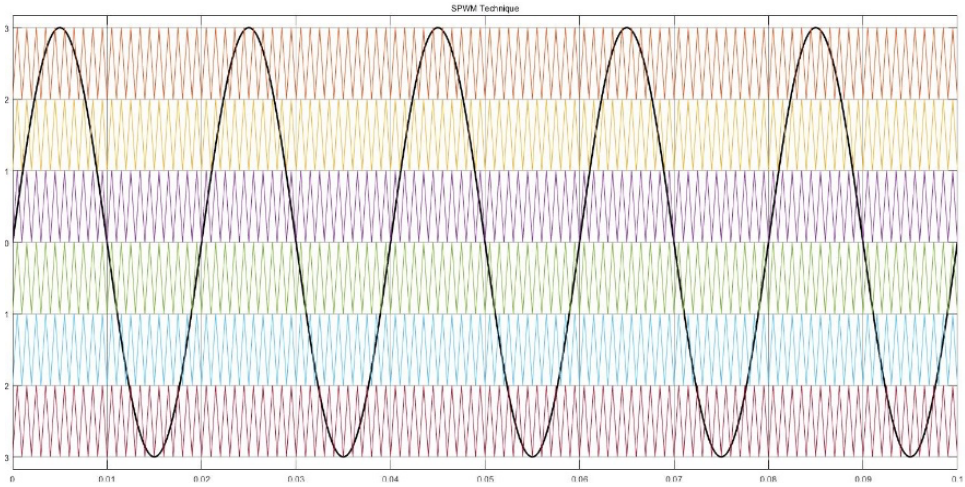


Figure 2. Ref signal wave with triangular carriers wave to make seven level SPWM

Illustrated in Figure 2, the process entails a comparison between the reference wave and the carrier waves, resulting in the creation of switching pulses designated for six individual switches. This comparison hinges on a logic differentiation: when the amplitude of the reference wave falls below that of the carrier wave, a logic value of 1 is assigned; conversely, when the reference wave amplitude exceeds that of the carrier wave, the logic value becomes 0. It is important to note that the reference wave assumes the form of a sine wave aligned with the desired output frequency, while the carrier wave takes the shape of a triangular waveform. For a visual depiction of the pulse generation for switches and the subsequent reference-carrier wave comparison, refer to Figure 3.

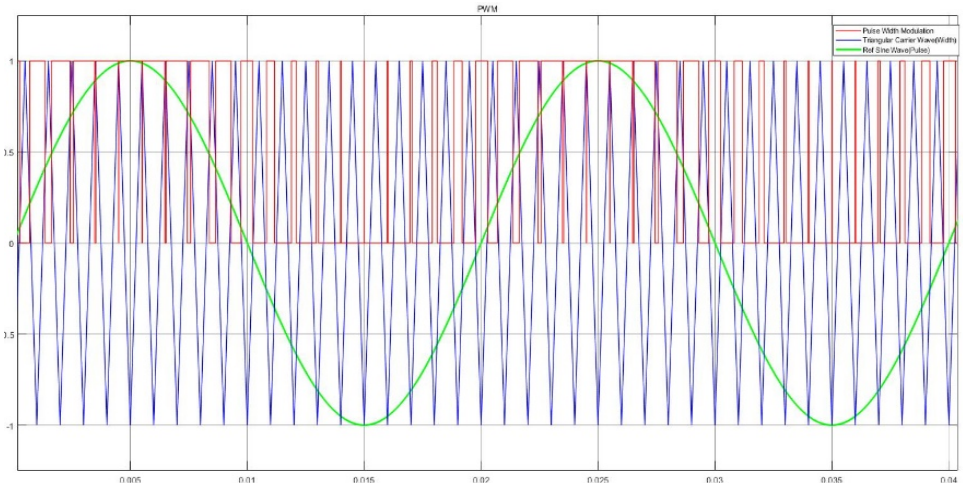


Figure 3. Comparison of the reference wave with the carrier wave to generate the switching pulses

The pulse applied to the switches is showcased in Figure 4. It is evident that the switching frequencies among the switches vary.

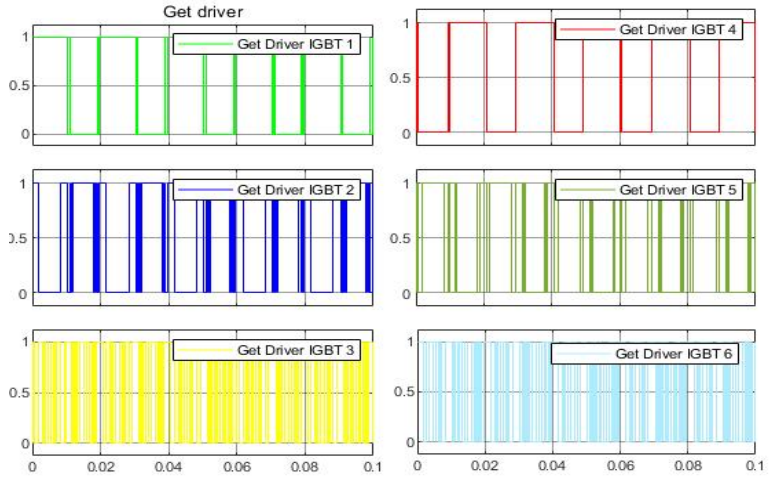


Figure 4. Applied pulses to the six inverter switches

For comprehensive guidance on the arrangement of switching and the formulation of output voltage levels, please refer to Table 2. As an illustrative example, when switches 1, 5, and 6 are activated, the cumulative voltage (V1) is engendered in the output. This operational principle extends to generate 7 distinct voltage levels in the output across various modes. It is pertinent to note that to prevent short circuits, the switches S4, S5, and S6 are configured as inverses of S1, S2, and S3, respectively. Consequently, only three switches is detailed in Table 2 and Figure 5, is portrays the block diagram representation of the proposed method.

Table 2. Switching state for one leg of the PUC-MLI

States	Voltages	*S1*	*S2*	*S3*
1	V1	1	0	0
2	V1-V2	1	0	1
3	V2	1	1	0
4	0	1	1	1
5	0	0	0	0
6	-V1	0	0	1
7	-V2-V1	0	1	0
8	-V2	0	1	1

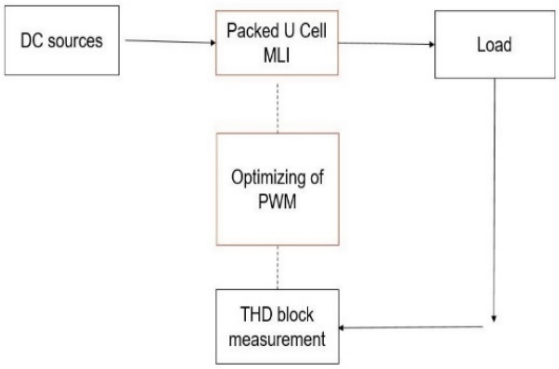


Figure 5. Block Diagram of the modification refers to [21]

The MPWM technique is visually depicted in Figure 6. This technique incorporates a dual-signal approach: a reference signal in the form of a sinusoidal waveform and an injected signal in the optimized sine waveform format. To tailor the parameters of the injected signal used in the SPWM approach, including amplitude, frequency, and phase-shifted angle, a process of optimization using WOA is employed. The expression for the injected signal's representation is articulated in equation 5, while the modified signal, as denoted in equation 6, is presented with reference to source [21].

$$v_i(t) = a_o * \sin(2 * \pi * f_o * t + \theta) \quad (5)$$

$$v_m(t) = 3 * \sin(2 * 3.14 * 50 * t + 0) + a_o * \sin(2 * \pi * f_o * t + \theta) \quad (6)$$

Where, $v_i(t)$ signifies the injected signal, wherein a_o represents the optimized amplitude, f_o denotes the optimized frequency, and Θ pertains to the optimized phase-shifted angle. The resultant modified signal, denoted as $v_m(t)$, materializes as a fusion between the reference signal and the injected signal.

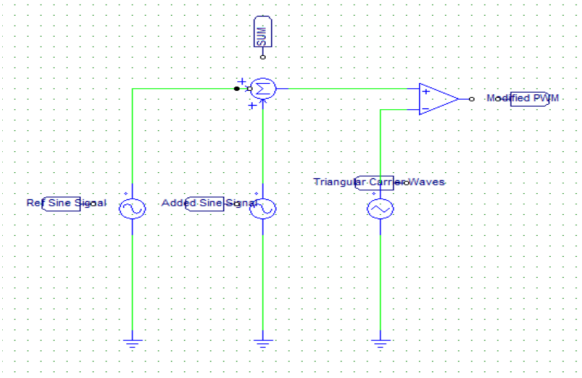


Figure 6. Schematic of the proposed method refers to [21]

c. Whale Optimization Algorithm

The adoption of meta-heuristic optimization algorithms continues to witness a notable upsurge within engineering applications. This escalating preference can be attributed to their reliance on concepts that are relatively straightforward, rendering their implementation comparably more manageable in contrast to alternative algorithms. What further sets them apart is their capability to operate without necessitating gradient information. Significantly, they also manage to sidestep the potential quagmire of becoming entrapped in local optimization minima. This versatility is especially appealing, as these algorithms find utility across an extensive gamut of problems spanning various disciplines. In the ensuing discussion, the WOA will be expounded upon.

Among the world's most colossal creatures, whales reign supreme, and the humpback whale is arguably the most renowned among the seven whale species. A fully-grown adult humpback whale can rival the dimensions of a typical school bus. These aquatic giants are avid pursuers of krill, which happens to be their preferred culinary delight. Krill, small aquatic organisms, are a staple in the diet of these whales. Remarkably, humpback whales exhibit a distinct and intriguing hunting method, which stands as a testament to their exceptional behavioral traits. This method, characterized by its exploratory nature, is widely recognized as the "bubble-net feeding method," as exemplified in Figure 7. The proposed algorithm contains of three steps which are siege hunting, exploitation phase (the method of attacking the web bubble) and discovery phase (search for prey). The flowchart of the proposed algorithm is shown in Figure 8. Based on the mentioned flowchart the WOA like all other meta-heuristic algorithms starts with the Initializing population, the next step is initializing parameters and then search for the best agent based on the following formula.

$$\vec{D} = |\vec{C} * \vec{X}^*(t) - \vec{X}(t)| \quad (7)$$

$$\vec{X}(t+1) = \vec{X}^*(t) - \vec{A} * \vec{D} \quad (8)$$

Where t represents the current iteration, $\vec{A}$ and $\vec{C}$ are coefficient vectors, X* is the location vector of the currently obtained best solution, and $\vec{X}$ is the location vector

refers to [24]. It should be noted that if there is a better solution, X* should be updated in each iteration. $\vec{A}$ and $\vec{C}$ vectors are calculated as follows:

$$\vec{A} = 2 * \vec{a} * \vec{r} - \vec{a} \quad (9)$$

$$\vec{C} = 2 * \vec{r} \quad (10)$$

Where $\vec{a}$ is linear from 2 to 0 and decreases during iterations (in both exploration and extraction phases) and $\vec{r}$ is a random vector in the interval from 0 to 1 refers to [24].

$$\vec{X}(\mathrm{t}+1) = \overrightarrow{D'}\mathrm{ebl.cos}\,(2\pi\mathrm{l}) + \vec{X}^*(\mathrm{t}) \quad (11)$$

Where $\overrightarrow{D'} = \vec{X}^*(\mathrm{t}) - \vec{X}(\mathrm{t})$ and indicates the distance of the ith whale to the prey (best solution obtained so far), b is a constant for defining the shape of the logarithmic spiral, l is a random number in [−1, 1], and is an element-by-element multiplication refers to [24].

$$\vec{X}(\mathrm{t}+1) = \begin{cases} \vec{X} * (\mathrm{t}) - \vec{A}.\vec{D} & \text{if } \mathrm{p} \le 0.5 \\ \overrightarrow{D'}.\mathrm{ebl.cos}\,(2\pi\mathrm{l}) + \vec{X} * (\mathrm{t}) & if\ p \ge 0.5 \end{cases} \quad (12)$$

Where p is a random number in [0, 1].

$$\vec{D} = |\vec{C} * \overrightarrow{X\mathrm{rand}} - \vec{X}| \quad (13)$$

$$\vec{X}(\mathrm{t}+1) = \overrightarrow{X\mathrm{rand}} - \vec{A} * \vec{D} \quad (14)$$

Where $\overrightarrow{X\mathrm{rand}}$ is a random position vector (a random whale) chosen from the current population refers to [24].

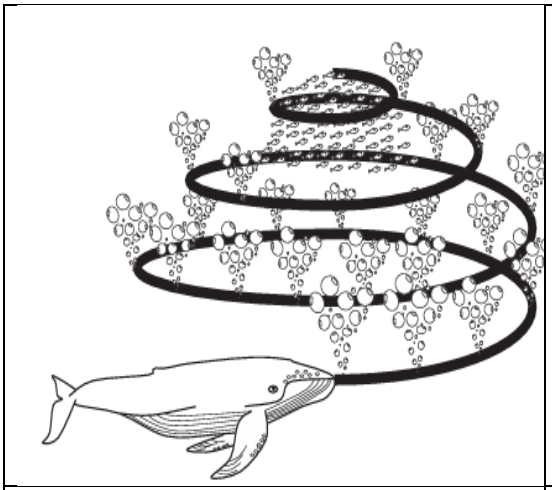


Figure 7. Whales hunting method refers to [24]

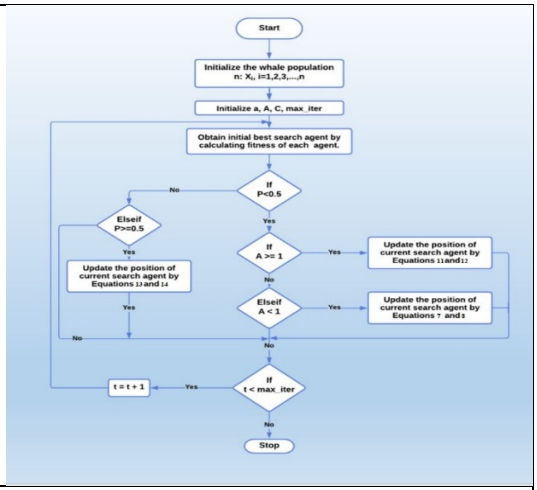


Figure 8. Follow-chart of the WOA

C. Result and Discussion

In this study, we conducted simulations of a densely packed u-cell multilevel inverter (PUC-MLI) using MATLAB-Simulink in an offline environment. Our proposed inverter was controlled through a custom PWM technique, and the specific parameters of the PUC-MLI used for this simulation are outlined in Table 3, where VDC1 was set to 33 volts and VDC2 to 11 volts. It is noteworthy that the presence of THD in the inverter's output voltage is directly associated with the particular switching sequence employed by its switches. In light of this observation, addressing THD required us to modify the inverter's switching sequence. To achieve this, we initially recorded the simulation data and meticulously verified its accuracy, designating it as our reference dataset. Subsequently, we introduced an auxiliary signal, referred to as the 'added signal,' which we combined with the reference signal. We then quantified the THD of the resulting composite signal. This 'added signal' incorporated three key parameters: amplitude, frequency, and phase shift angle, all of which played pivotal roles in optimizing the inverter's switching sequence.

To optimize these parameters, we employed a WOA that randomly assigned values to each parameter within predefined bounds and assessed the resulting THD of the combined signal. If the THD exceeded that of the previous iteration, the candidates were eliminated. Conversely, if the THD was lower, we retained and presented the best candidate values at the conclusion of each iteration. In order to avoid getting stuck in local optima and find the global optimum, we ran the algorithm with standard settings 100 times. The process of searching for the global optimum is depicted in Figure 9. As shown in Figure 9, the global optimum for the proposed algorithm is 12.44% THD, which is highlighted with green barchart, the red barchart indicates the THD values higher than SPWM that means error and blue barchart means a solution for the problem however, not best solution (local optima). The primary goal of using the optimization algorithm is to reduce THD. The WOA was implemented using the Python programming language within the Visual Studio Code (VSC) environment.

Figure 10 provides a visual representation of the tracking process for the parameter transitions from Figure 10(a) to Figure 10(c), while Figure 10-(d) illustrates the evolution of THD across iterations. Our proposed algorithm demonstrated substantial success in reducing THD, yielding noteworthy results. Specifically, it identified optimal values for amplitude [a = 0.3488108583915273], frequency [f =999.2244623906344], and phase shift angle [theta = 4.95808221801622], resulting in a remarkable reduction in THD from 17.89% to 12.44%, a highly favorable outcome. These findings are detailed in Table 4.

Table 3. PUC-MLI simulation parameters

Components	*Value*
VDC1	33
VDC2	11

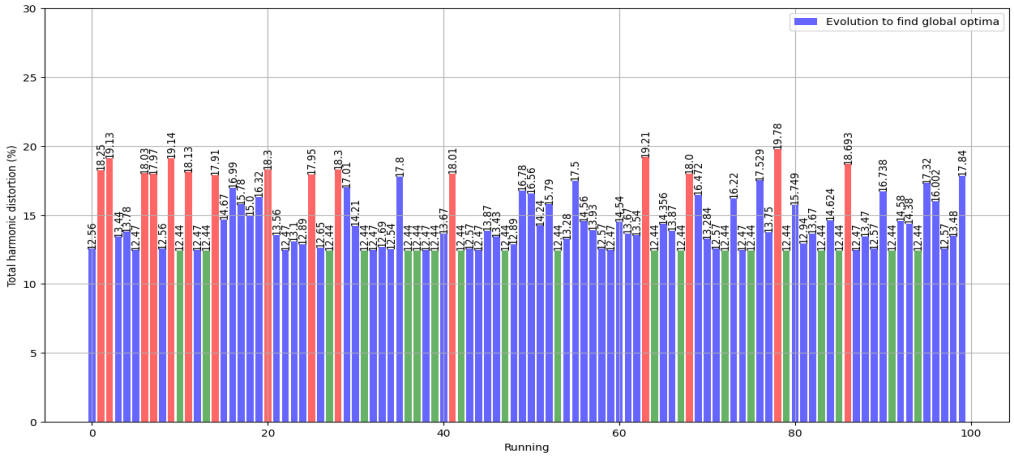
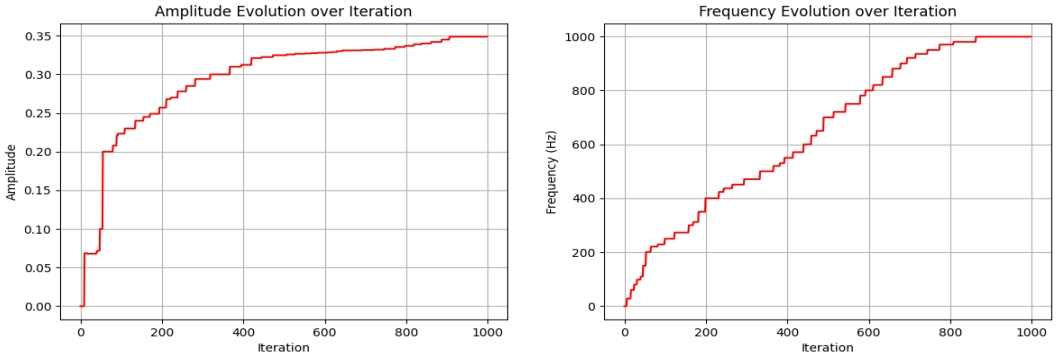
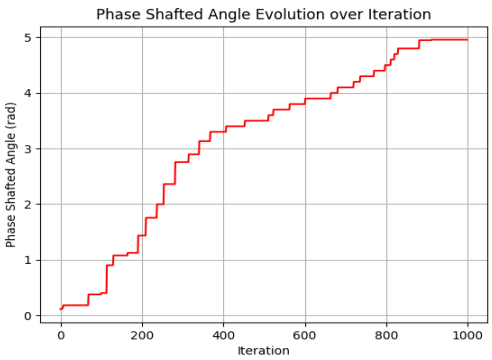


Figure 9. Evolution of finding global optima

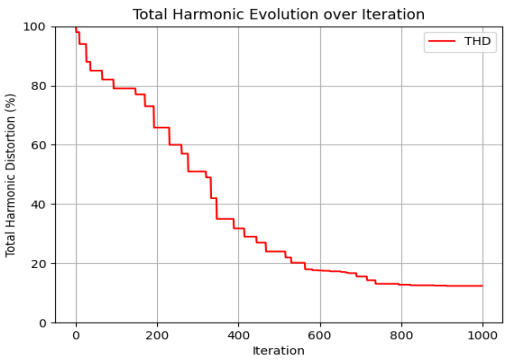


(a)

(b)



(c)



(d)

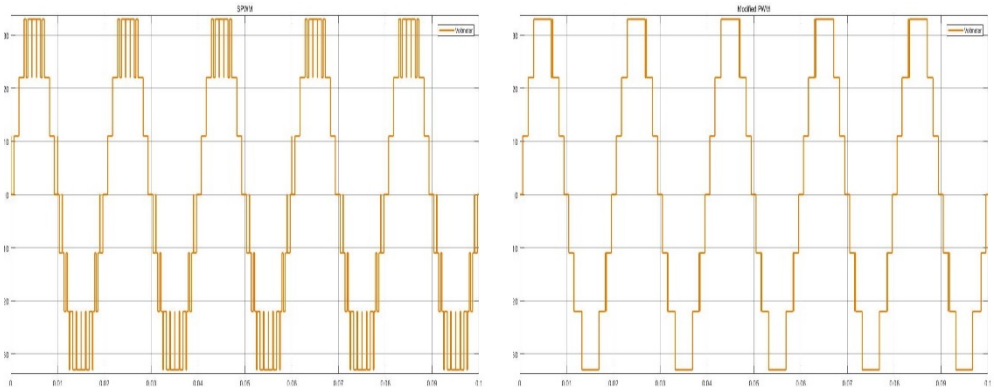
Figure 10. The modification process, **Figure 10(a)** amplitude, **Figure 10(b)** frequency, **Figure 10(c)** phase shafted angle, and **Figure 10(d)** total harmonic distortion

The comparison of output voltage waveforms for the PUC-MLI using both SPWM and MPWM techniques was conducted using MATLAB software. Figure 11 provides a visual representation, transitioning from Figure 11(a) depicting the output voltage in the SPWM configuration to Figure 11(b) showing the output voltage in the MPWM configuration. It is important to note that both SPWM and MPWM employed the same amplitude modulation.

Table 4 presents a concise summary of the THD levels observed in the PUC-MLI for both SPWM and MPWM. The THD for SPWM was measured at 17.89%, while MPWM demonstrated a reduced THD level of 12.44%. For a deeper understanding of the harmonic content, Figure 12(a) illustrates the harmonic spectrum of SPWM, while Figure 12(b) displays the harmonic spectrum of MPWM.

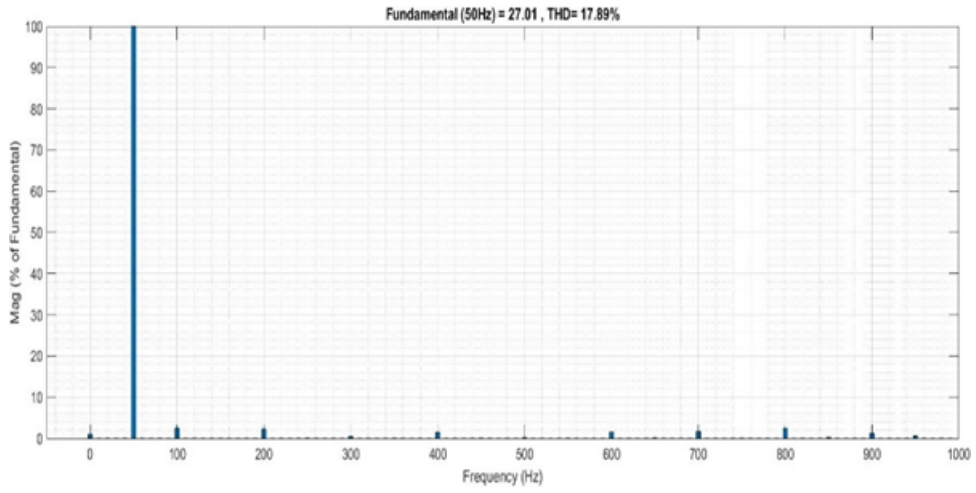
Table 4. THD comparison between SPWM and MPWM

Components	***Value***
SPWM	17.89%
Modified PWM	12.44%

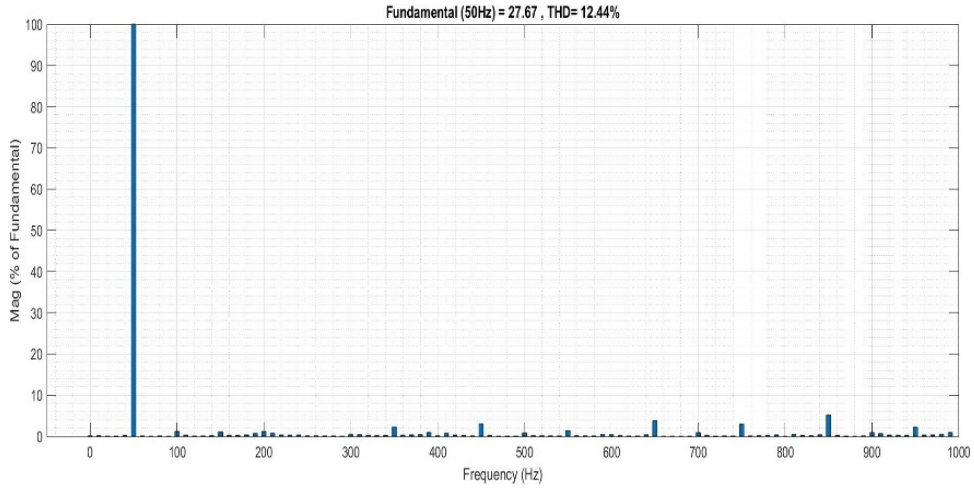


(a) (b)

Figure 11. Output voltage of the inverter, **Figure 11(a)** SPWM and **Figure 11(b)** MPWM



(a)



(b)

Figure 12. Result of FFT analysis: **Figure 12(a)** THD spectrum of SPWM and **Figure 12(b)** THD spectrum of the MPWM

D. Conclusion

In this research, we applied whale optimization algorithm to optimize the switching patterns of the inverter's switches with the objective of minimizing total harmonic distortion in the output voltage. The results illustrated the effectiveness of whale optimization algorithm, achieving a considerable reduction in total harmonic distortion, notably from 17.89% to 12.44%. This method stands out for its cost efficiency in improving the total harmonic distortion of an inverter's output voltage. Moreover, its adaptability is noteworthy, as it is applicable across a range of multilevel inverter configurations, regardless of the varying output voltage levels, highlighting its broad utility.

E. References

[1] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous power theory and applications to power conditioning," IEEE Transactions on Industry Applications, vol. IA-20, no. 3, pp. 624-630, 1984.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, 2002.

[3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, et al., "Recent advances and industrial applications of multilevel converters," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, 2010.

[4] H. Abu-Rub, A. Iqbal, and M. Malinowski, "A comprehensive review of hybrid multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1088-1105, 2011.

[5] X. Li, Y. Li, J. Li, and Y. Sun, "Voltage Distortion of Multi-level Inverters and Its Mitigation," in 2019 IEEE 9th International Conference on Electronics Information and Emergency Communication (ICEIEC), 2019, pp. 1-4.
[6] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," IEEE Transactions on Industry Applications, vol. 32, no. 3, pp. 509-517, 1996.
[7] A. M. Bazzi, Z. M. Salameh, and T. A. Lipo, "A novel family of multilevel inverters," IEEE Transactions on Industry Applications, vol. 33, no. 2, pp. 518-525, 1997.
[8] Y. Liu and H. Abu-Rub, "Multilevel dc-dc converters: A review," IEEE Transactions on Industrial Electronics, vol. 60, no. 7, pp. 2786-2797, 2013.
[9] F. Z. Peng, "Z-source inverter," IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 504-510, 2003.
[10] A. Davoudi and H. Farzanehfard, "An optimal pulse width modulation technique using genetic algorithms," in 2011 IEEE Power and Energy Society General Meeting, 2011, pp. 1-6.
[11] E. Rashedi, H. Nezamabadi-pour, and S. Saryazdi, "GSA: A gravitational search algorithm," Information Sciences, vol. 179, no. 13, pp. 2232-2248, 2009.
[12] M. Salimi, M. Moeini-Aghtaie, and B. Mohammadi-Ivatloo, "Multi-objective optimization of a microgrid using a hybrid firefly-genetic algorithm," Energy Conversion and Management, vol. 91, pp. 39-49, 2015.
[13] Aala Kalananda Vamsi Krishna Reddy and Komanapalli Venkata Lakshmi Narayana, "Optimal total harmonic distortion minimization in multilevel inverter using improved whale optimization algorithm," International Journal of Emerging Electric Power Systems, vol. 21, no. 3, 2020, pp. 20200008. doi: 10.1515/ijeeps-2020-0008.
[14] P. D. P. Reddy, V. C. V. Reddy, and T. G. Manohar, "Whale optimization algorithm for optimal sizing of renewable resources for loss reduction in distribution systems," Renewables, vol. 4, no. 3, 2017. doi: 10.1186/s40807-017-0040-1.
[15] M. Naseri, V. Ahmadifard, and H. Sadeghi, "Comparison of Cascaded H-Bridge and Packed U-Cell Multilevel Inverters in the Context of Reactive Power Compensation," IEEE Access, vol. 8, pp. 109756-109766, 2020.
[16] W. Zhang, X. He, Q. Wang, and J. Wu, "A New Space Vector Modulation Strategy for Packed U-Cell Modular Multilevel Converters," IEEE Transactions on Power Electronics, vol. 34, no. 11, pp. 10547-10561, 2019.
[17] F. Hamzehlouia and S. H. Hosseini, "Design and Analysis of a Packed U-Cell Multilevel Inverter Using a Hybrid Method of Particle Swarm Optimization and Teaching-Learning-Based Optimization," IEEE Access, vol. 7, pp. 138129-138141, 2019.
[18] Y. Wang, Y. Zhang, and L. Shao, "An Improved Packed U-Cell Modular Multilevel Converter for Photovoltaic Systems," in 2020 IEEE 4th International Conference on Energy Internet (ICEI), 2020, pp. 64-68.
[19] M. Salman, I. U. Haq, T. Ahmad, et al., "Minimization of total harmonic distortions of cascaded H-bridge multilevel inverter by utilizing bio inspired AI algorithm," J Wireless Com Network, vol. 66, 2020. doi: 10.1186/s13638-020-01686-5.

[20] M. A. Al-Mamun, M. A. Hannan, M. A. Hossain, and M. A. Islam, "Comparison of GA and PSO Optimized Switching Angles for 3-phase 15-Level Asymmetrical Multilevel Inverter," in Proceedings of the 11th International Conference on Robotics, Vision, Signal Processing and Power Applications, Feb. 2022, pp. 399-404. doi: 10.1007/978-981-16-8129-5_62.

[21] F. Ebrahimi, N. A. Windarko, and A. I. Gunawan, "Reducing THD of 7-Level Packed U-cell Multilevel Inverter Using Genetic Algorithm," 2023 International Electronics Symposium (IES), Denpasar, Indonesia, 2023, pp. 88-93. doi: 10.1109/IES59143.2023.10242460.

[22] H. Vahedi and K. Al-Haddad, "Method and system for operating a multilevel inverter," US Patent 20160126862, May 5, 2015. doi: N/A.

[23] K. Sheela and K. R. Mohan, "Modified PUC Multilevel Inverter Topology with Reduced Switching Components," IEEE Transactions on Power Electronics, vol. 31, no. 3, pp. 2088-2099, March 2016. doi: 10.1109/TPEL.2015.2434425.

[24] S. Mirjalili and A. Lewis, "The Whale Optimization Algorithm," in Advances in Engineering Software, vol. 95, pp. 51-67, 2016. doi: 10.1016/j.advengsoft.2016.01.008.